Pore Formation Study in Porous Nanocrystalline Silicon Membrane

by

Chengzhu Qi

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Professor Philippe M. Fauchet

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Biographical Sketch

The author was born in Zhashui, Shaanxi, China, in 1984. He attended Xi'an University of Architecture and Technology, and graduated with a Bachelor of Science degree in Materials Science and Engineering in 2006. He then attended Xi'an Jiaotong University, and graduated with a Master of Science degree in Materials Science in 2009. He started his doctoral studies in Materials Science at the University of Rochester in 2010. He was awarded a NYSERDA Scholarship in 2010 and received his second Master of Science degree from the University of Rochester in 2012. His doctoral work focuses on research and development of porous nanocrystalline silicon membrane, under the direction of Professor Philippe Fauchet in the Department of Electrical and Computer Engineering.

The following publications and presentations were a result of work conducted during doctoral study:

C. Qi, C. C. Striemer, T. R. Gaborski, J. L. McGrath, P. M. Fauchet, Highly Porous Silicon Membranes Fabricated from Silicon Nitride/Silicon Stacks, *Small*, DOI: 10.1002/smll.201303447

C. Qi, D. Z. Fang, C. C. Striemer, J. L. McGrath, P. M. Fauchet, Influence from the Silicon Dioxide Capping Layers on Porous Nanocrystalline Silicon Membrane, submitted to *Nanoscale*.

C. Qi, C. C. Striemer, T. R. Gaborski, J. L. McGrath, P. M. Fauchet, TEM Observation of

Pore Formation during In-situ Heating in Silicon Nitride/Silicon Stacks, in preparation for submission.

C. Qi, C. C. Striemer, T. R. Gaborski, J. L. McGrath, P. M. Fauchet, Pore Shape Control in Porous Nanocrystalline Silicon Membrane, contribute talk at 2014 Spring MRS Meeting, San Francisco, 2014.

C. Qi, C. C. Striemer, T. R. Gaborski, J. L. McGrath, P. M. Fauchet, *Highly Tunable Porous Silicon Membrane from Si_3N_4/ Si/ Si_3N_4 Stack*, contributed talk at 2013 Spring MRS Meeting, San Francisco, 2013.

C. Qi, C. C. Striemer, J. L. McGrath, P. M. Fauchet, *Ultra-high Porous Silicon Membrane from Silicon Nitride/ Silicon/ Silicon Nitride Stacks*, poster presentation at 2012 Fall MRS Meeting, Boston, 2012.

C. Qi, D. Z. Fang, C. C. Striemer, J. L. McGrath, P. M. Fauchet, *Transition from Pore Formation to Agglomeration after Annealing of Ultrathin Amorphous Silicon Films Sandwiched between Ultrathin Silicon Dioxide Layers*, contributed talk at 2012 Spring MRS Meeting, San Francisco, 2012.

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Abstract

Porous nanocrystalline silicon (pnc-Si) membrane is a new class of materials that is promising for a wide range of applications from biofiltration to cell culture substrate. Nano-size pores are spontaneously formed in a silicon film sandwiched between two silicon dioxide layers during rapid thermal annealing. Previous research has shown that pore formation in the pnc-Si membrane is thermally driven and closely connected to silicon crystallization, however, the process by which pore are formed is still not well understood.

In this thesis, the fabrication and characterization process of pnc-Si membranes is first introduced to understand their basic structure and properties, followed next by a study on the effects silicon dioxide capping films have on pore formation. The results show that both the top and bottom silicon dioxide films are essential to pore formation in pnc-Si membranes. The top oxide layer prevents the silicon film from agglomerating while the bottom oxide layer acts as a barrier layer to prevent homoepitaxy of the silicon film during annealing.

To study the effects of capping materials on pore formation, silicon nitride, is incorporated into the sandwich structure to replace the capping silicon dioxide layers. From this study, it was found for the first time that nanopores can still be formed in silicon films sandwiched between two silicon nitride layers during rapid thermal annealing. Pore formation in these new silicon nitride capped structures is then discussed, along with the resulting pore characteristics.

In the final part of this thesis, ex-situ and in-situ annealing studies of pore formation in pnc-Si membranes are discussed. The ex-situ study shows that both the silicon crystallization and associated pore formation are enhanced in the silicon film in the nitride/silicon/nitride (NSN) stack compared to that in the oxide/silicon/oxide (OSO) stack. The in-situ heating studies demonstrate that pore growth in the NSN stack follows a pearl-necklace pattern while no clear pattern is observed from the OSO stack. The energy-dispersive X-ray spectroscopy (EDS) study shows that Ar atoms embedded during sputtering move together, forming Ar bubbles to occupy the porous areas in the silicon film during the heating process. These Ar bubbles are held in the pores of the silicon film when silicon nitride is used to cap the membrane, but when silicon dioxide is used as the capping layer the Ar diffuses out of the structure. This may lead to the different pore growth patterns between the NSN and OSO stacks. Finally, pore formation process can be understood in two stages which are void nucleation and pore growth. Nano-voids are nucleated in the silicon film near interface with the oxide or nitride layer, and grow in both the vertical and lateral directions during crystallization process. This process is attributed to the diffusion of silicon atoms during the transition from amorphous silicon to nanocrystalline silicon. These voids become through pores when their growth spans the entire silicon film in the vertical direction. The pore growth is strongly affected by the silicon thickness, temperature ramp rate and capping layers.

Contributor and Funding Sources

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List of Acronym

Acronym	Full Name
SEM	Scanning electron microscopy
TEM	Transmission electron microscopy
AFM	Atomic force microscopy
APD	Average pore diameter
NSN	Nitride/ silicon/ nitride stack
NSO	Nitride/ silicon/ oxide stack
OSN	Oxide/ silicon/ nitride stack
OSO	Oxide/ silicon/ oxide stack
PNC-Si	Porous nanocrystalline silicon membrane
EDS	Energy-dispersive X-ray spectroscopy
TE	Track-etched
AAO	Anodic aluminum oxide
CNT	Carbon nanotube
RIE	Reactive ion etch
FIB	Focused ion beam
HAADF	High angle annular dark field

Chapter 1 Introduction

1.1 Introduction to porous membranes

A membrane is normally defined as a physical barrier allowing selective transport of mass. Membranes are widely used for separation and purification in many industrial applications. Membranes can be classified into different categories based on the pore geometries, materials, and fabrication techniques. According to the IUPAC (International Union of Pure and Applied Chemistry), porous membranes groups are called microporous (<2μm), mesoporous (2-50μm) and macroporous (>50μm) based on the pore size [1]. Based on the membrane material, they can be classified as organic, inorganic or hybrids of organic/inorganic systems. Membranes can also be classified by their fabrication technique, such as track-etched membrane, anodic aluminum oxide membrane, carbon nanotube membrane, nanoporous silicon nitride membrane and so on. Porous nanocrystalline silicon membranes, which were developed at the University of Rochester in 2007, will be discussed in detail in the following sections.

1.1.1 Track-etched (TE) membrane

The production of porous membranes by utilizing the nuclear tracks was proposed almost immediately after the discovery of particle track etching in thin sheets of materials [2]. This technique was used by industry quickly. There are two basic methods to produce track-etched membranes. The first method is by irradiation of polymeric sheets, micas, and

glasses with fragments from the fission of heavy nuclei such as californium or uranium [2, 3].The second method makes use of heavy ion beams, usually with an energy on the order of several MeV, produced by accelerators [3-10]. Chemical etching is used after the irradiation to create the pores. During chemical etching the damaged zone of a latent track is removed and transformed into a hollow channel [2, 3]. The exposure time of the membrane to the ion bombardment determines the number of pores, and the etch duration controls the size of the pores. Polycarbonate, polyester or polyethylene terephthalate are used as base polymer material [11-13].

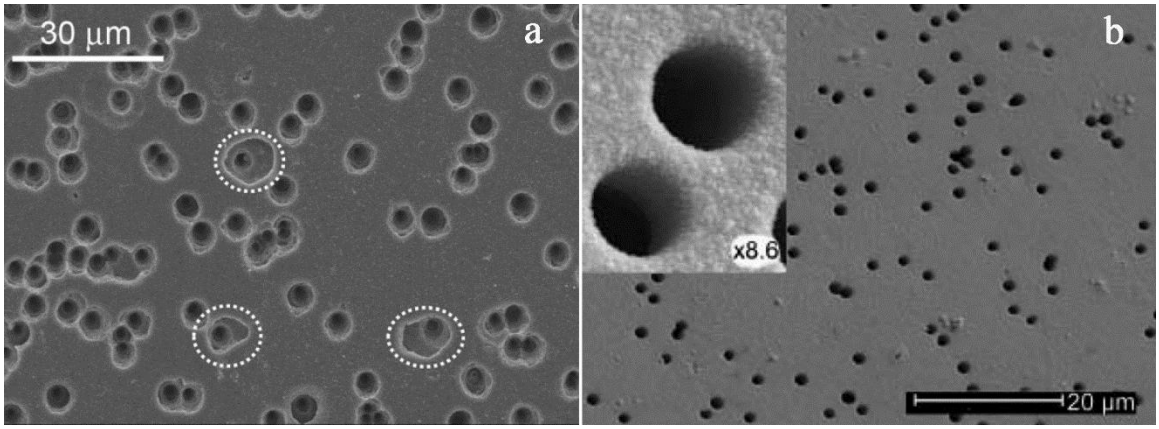


Figure 1-1 A few examples of porous track-etched membrane, (a) Field emission scanning electron microscope (FESEM) image of etched poly(ethylene terephthalate) membrane from [14], and (b) SEM image of track-etched membrane from [15].

Figure 1-1 shows two examples of porous structures produced on thin polymeric films using various methods of irradiation and chemical treatment. Track-etched membranes are typically 100 μm – 1000 μm thick with average pore sizes ranging from

10 nm – 100 nm and porosities that approach 10%. The main application of commercially produced track membranes is for process filtration, cell culture and laboratory filtration.

Track-etched membranes offer distinct advantages over conventional membranes due to their precisely determined structure, such as pore size, shape and density. However, they have several disadvantages. First is the temperature limit. They cannot withstand temperatures above 130 ℃, which greatly limits their range of applicability. The low chemical stability and structural weakness are two other issues that TE membranes have get to solve.

1.1.2 Anodic aluminum oxide (AAO) membrane

The AAO membrane is produced by using an electro-chemical process to anodize aluminum in acid solutions. During this process a self-organized, highly ordered array of cylindrical shaped pores can be produced with controllable pore diameters, periodicity and density distribution [16]. The AAO membranes can be used as templates in a variety of nanotechnology applications, such as nanorods and quantum dots growth, eliminating the need for expensive nanolithography techniques. The SEM image of figure 1-2 shows the morphology and cross section of an AAO membrane.

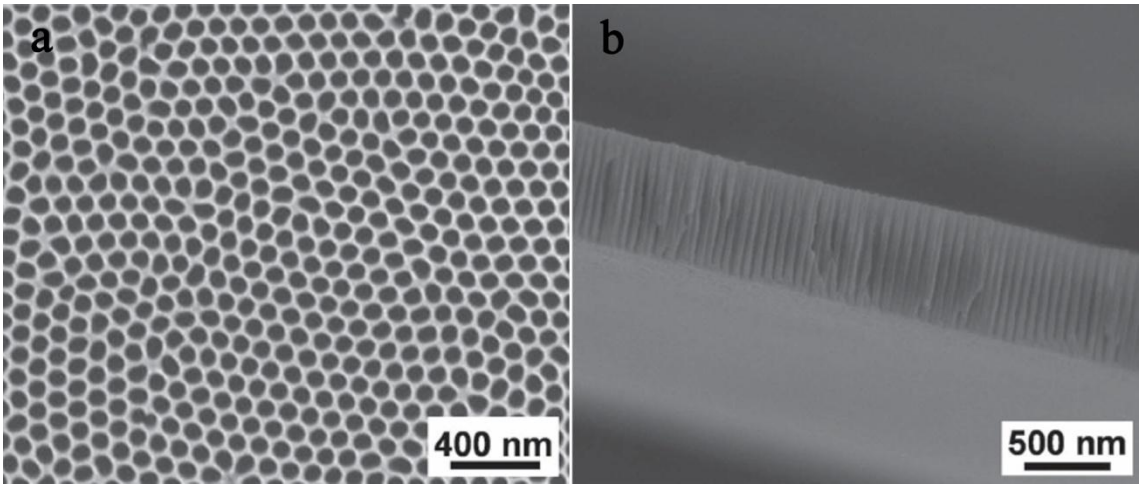


Figure 1-2 SEM images of an AAO nanoporous membrane with a) top down view and, b) cross section view [15].

A variety of acids have been used in the aluminum anodization process. The acids that are commonly using include oxalic acid, phosphoric acid, and sulfuric acid. Other acids that have been used are malonic and citric acids, which can also produce a regular pore arrangement under specific anodizing conditions [17]. The resulting pore diameters can range in size from 4 to 250 nm [18, 19] and the inter-pore distance can range from 50 to 420 nm [20, 21]. The thickness of the AAO membranes can vary from several hundred nanometers to several microns [22].

Al anodization is a relatively inexpensive and controllable electro-chemical process. Both the chemical stability and temperature endurance of AAO membranes is much better than that of TE membranes. However, brittleness is a big concern for AAO membranes, which limits their use in some applications. The permeability is also limited by the thickness of AAO membranes.

1.1.3 Carbon nanotube (CNT) membrane

Carbon nanotubes (CNTs) are nanoscale cylinders of graphene with exceptional properties such as high mechanical strength, high aspect ratio and large specific surface area [23]. As a result, CNTs based membranes have attracted a lot of interest in recent years.

A continuous membrane structure can be obtained by filling the spaces between the CNTs with a continuous polymer or inorganic matrix and opening the closed end of the nanotubes by etching [24]. Kim *et al*. [25] filtrated aligned single-walled CNTs with a poly (tetrafluoroethylene) filter and sealed the CNTs with polysulfone polymer. Their membranes showed the same fast gas transport properties as those observed in CNT membranes grown by chemical vapor deposition. Other groups [26, 27] have shown the vertical-aligned carbon nanotubes with high gas flow rate. However, these CNT-based membranes have low porosity. As a result, the gas permeabilities of whole membranes were limited because of the low porosity. Yu *et al.* demonstrated densely packed CNT membranes with a porosity of 20% without the use of a filler polymer (see Figure 1-3). However, their CNTs were 3nm in diameter and no extension of this approach to larger tube diameters [28]. The complicated fabrication process is another limit of the CNT membranes.

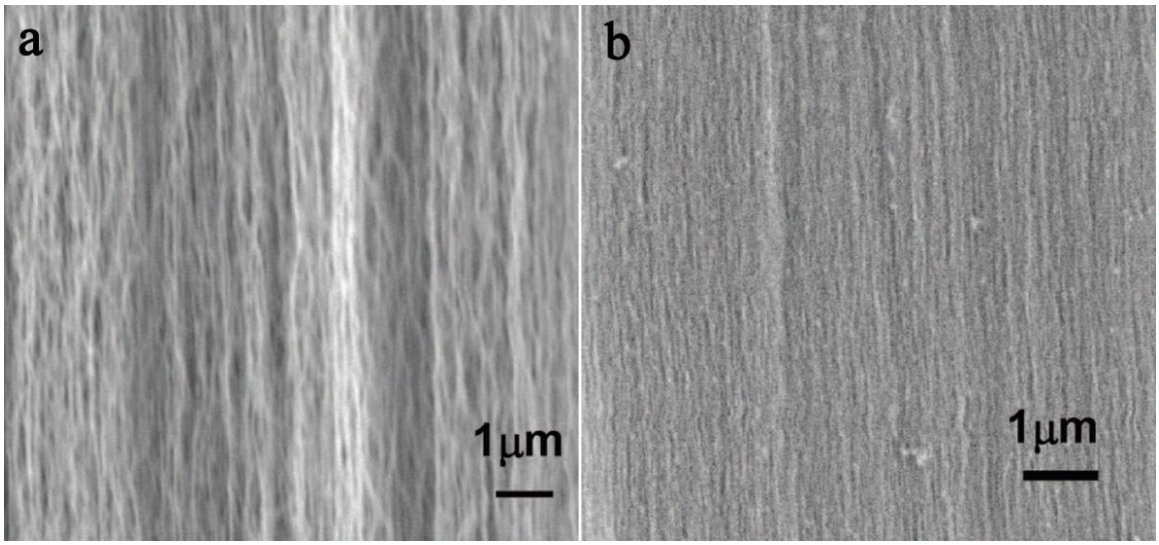


Figure 1-3 (a) SEM image of the cross section of vertically aligned CNTs, (b) SEM image of the cross section of a dense CNT membrane [27].

1.1.4 Nanoporous silicon nitride (SiN) membrane

Nanoporous SiN membranes have raised great interest in recent years thanks to the development of advanced nanolithography techniques. The nanopores are often machined in a suspended low stress SiN membrane [29-35] thanks to the excellent thermal stability and chemical inertness of SiN. So far, electron beam lithography followed by reactive ion etching (RIE) [33, 34] or focus ion beam (FIB) etching [29-32] have been used to create pores in the SiN membrane. Tong *et al.* demonstrated ultrathin SiN nanosieve membranes with uniform cylindrical pores and pore diameters using FIB etching [36]. Meller *et al.* also showed that the pore size in ultrathin freestanding SiN membranes is mainly affected by the FIB current and dwelling time [37].

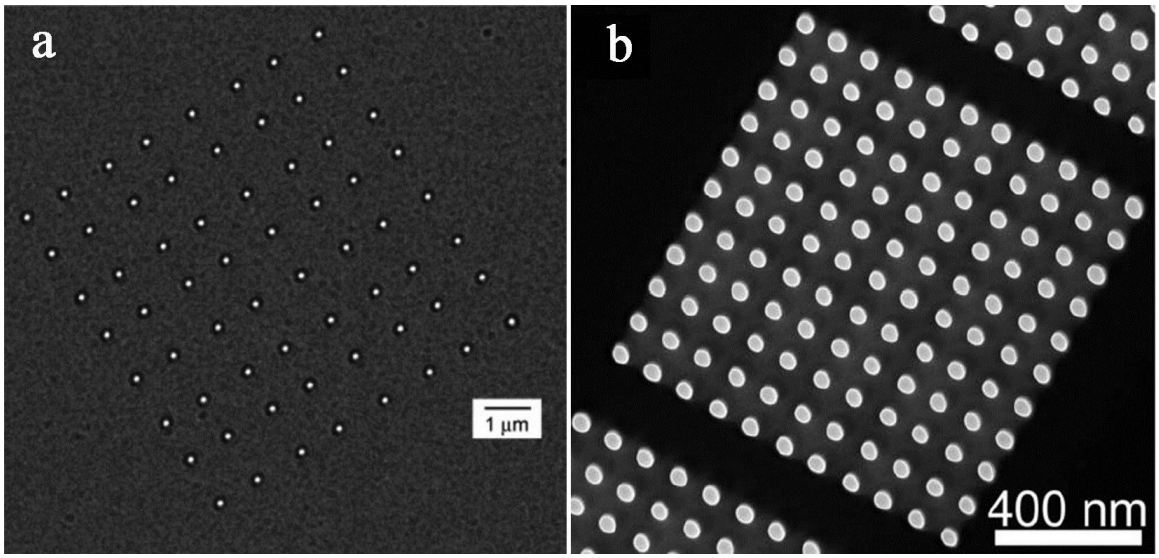


Figure 1-4 (a) TEM image of nanoporous SiN membrane fabricated using FIB from [37], (b) TEM image of FIB milled array of pores drilled through a SiN membrane from [38].

The major advantage of this nanoporous SiN membrane is that both the pore size and the porosity can be precisely controlled by the electron beam or FIB etching (see Figure 1-4). However, disadvantages, including long processing time and very high cost, make it difficult for scaled-up production.

1.1.5 Ultrathin porous nanocrystalline silicon membrane

Porous nanocrystalline silicon (pnc-Si) membrane is a new class of materials that exhibits a lot of remarkable properties such as high permeability [39, 40], biocompatibility [42] and pore size tenability [43]. Pnc-Si is promising for a wide range of applications including biofiltration, gas separation, sensing (pressure, temperature, biological) [41] and

cell culture [42]. Figure 1-5 (a) is a scanning electron microscopic (SEM) image of a 15nm thick pnc-Si membrane. Figure 1-5 (b) shows a transmission electron microscopic (TEM) image of a membrane. The white dots represent pores and the black dots represent the silicon nanocrystals.

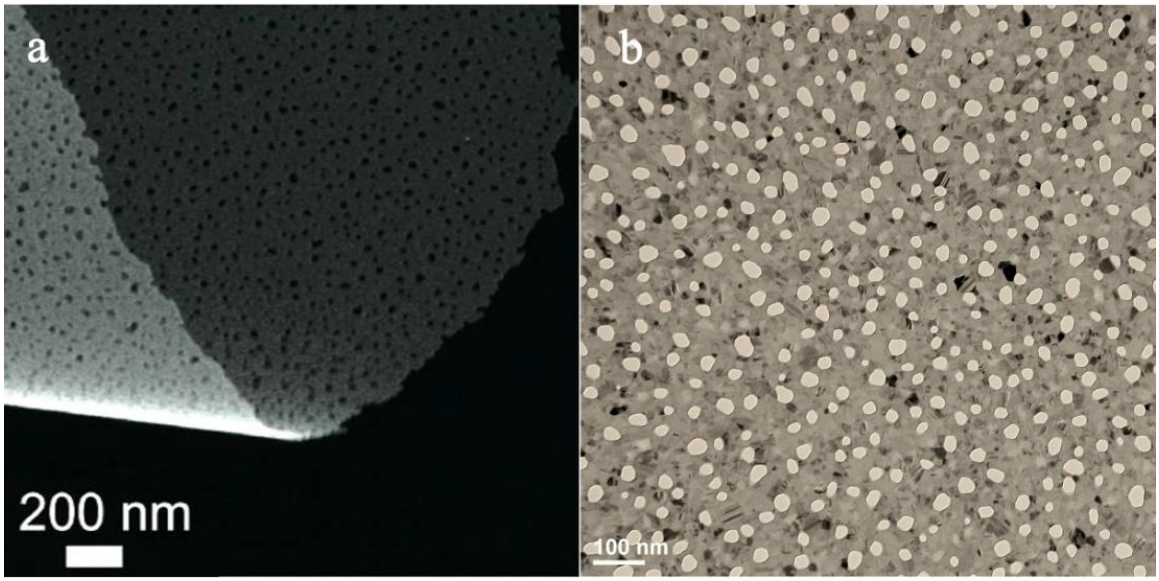


Figure 1-5 (a) SEM image of a 15nm thick pnc-Si membrane [58], and (b) TEM image of pnc-Si membrane where white dots are pores and black dots are silicon crystals.

1.2 Advantages and progress of pnc-Si membrane

Pnc-Si membranes have shown many advantages compared with polymeric membranes. Commercial nanoporous polymer membranes are typically made up of small bumps, or nodules. The pores between the nodules are 1- 50 nm across. The thickness of this type membrane is normally 500 nm. One tradeoff for this polymer membrane is that

the flux is significant restricted by thickness and tortuous pathway through the membrane [47]. This tradeoff is addressed by the ultra-thin nature of pnc-Si (see Figure 1-6).

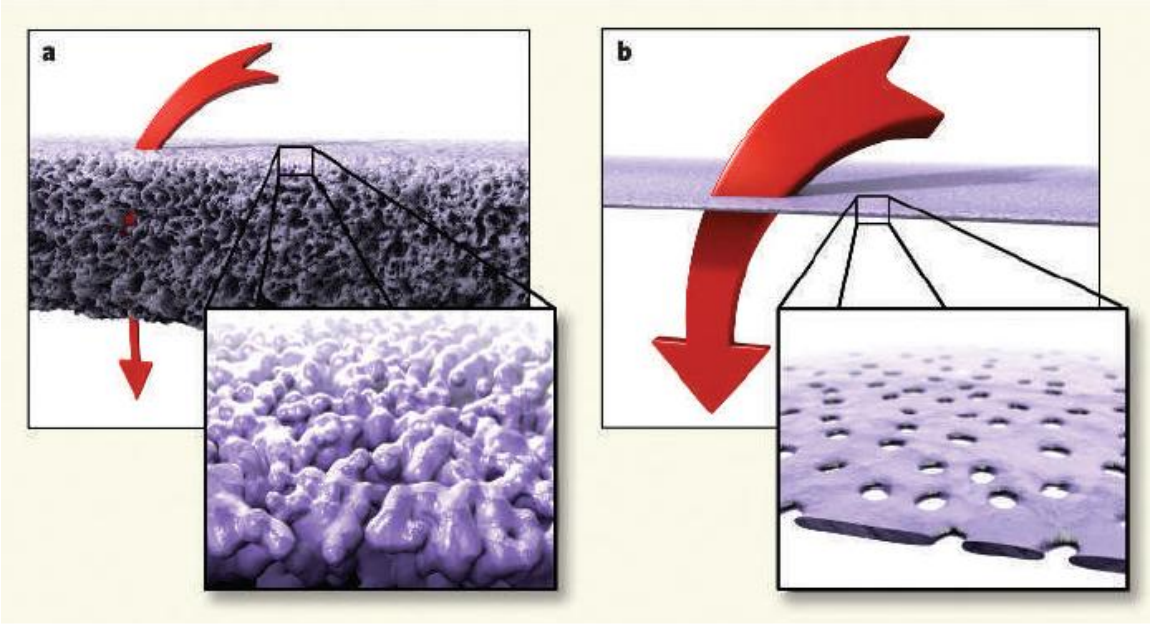


Figure 1-6 Comparison of sponge- like and ultra-thin porous membrane geometries: a) conventional polymer membrane significantly hinders the flow; b) an ultrathin porous nanocrystalline silicon (pnc-Si) membrane has almost no resistance to the flow [44, 47].

The typical thickness of pnc-Si membranes is around 15nm with pore size from 5-80nm and porosity from less than 1% to 15%. The flow through the pnc-Si membrane is enhanced by the large size of pores and also by the ultra-thin nature of this membrane compared with the polymer porous membrane. Table 1-1 summarizes the pore size and thickness range of porous membranes.

Table 1-1 Pore size and thickness range of porous membranes

Membrane	Thickness (nm)	Pore size (nm)	References
TE	10^5-10^6	10-100	[11-15]
AAO	10^2-10^3	4-250	[18, 19, 22]
CNT	750	1-5	[28]
SiN	10-270	25-100	[36-38]
Porous polymer	500	1-50	[47]
Pnc-Si	15-30	5-80	[43, 44]

Another advantage of pnc-Si membranes is that they can easily and inexpensively be manufactured using a standard semiconductor fabrication techniques, which enables scale-up production (Figure 1-7). Other methods to make ultrathin nanorporous membranes either use sophisticated nanolithography techniques or colloidal templates [36, 45]. The nanolithography approach is too expensive for large scale production and the second approach is limited in pore sizes. In pnc-Si membranes, the pore size can be tuned by the annealing temperature, deposition condition, temperature ramp rate and other factors.

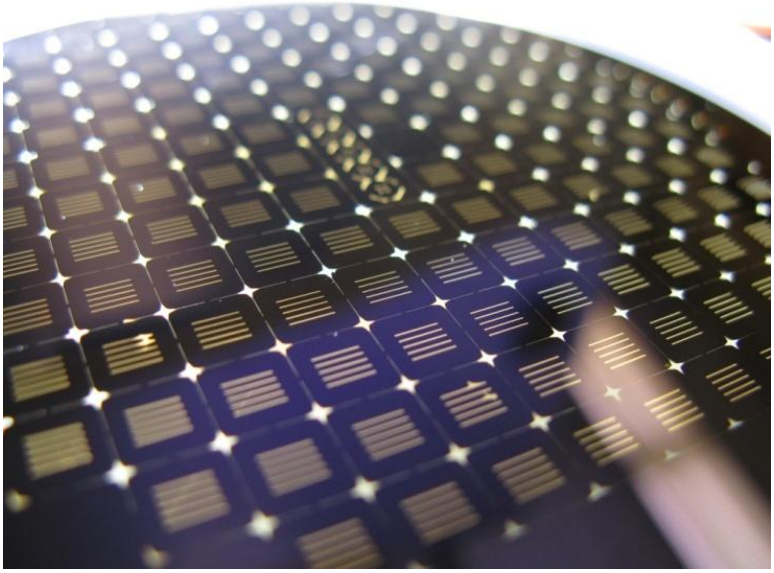


Figure 1-7 Hundreds of membrane "chips" can be produced on a single 4-inch silicon wafer. The golden rectangular features are areas of free-standing pnc-Si membrane [43].

A third advantage of pnc-Si membranes is that they are easy to integrate into a 'lab-on-a-chip' microfluidic system, which is attractive for medical diagnostics, drug discovery and chemical synthesis [46, 48].

Significant progress has been made since the first report on pnc-Si membranes. A recent study by Agrawal *et al.* [42] showed pnc-Si membranes can be used as highly permeable and molecularly thin substrates for cell culture. Their results demonstrate that cells can be grown and survive on pnc-Si membranes and that pnc-Si membranes are biodegradable.

Separation of nanoparticles using pnc-Si membranes has been studied by Gaborski *et al.* [49]. Their results showed that pnc-Si membrane can fractionate gold nanoparticles

with better than 5nm resolution and insignificant sample loss. Their measured water permeability is orders of magnitude higher than those exhibited by commercial ultrafiltration and experimental carbon nanotube membranes.

Factors that affect the pore morphology in pnc-Si membrane were explored by Fang *et al.* [43]. They showed that pore size and porosity can be tuned by varying silicon film thickness, annealing temperature, annealing time, and thermal ramp up rate. Fang *et al.* further explored the carbonization of pnc-Si membranes [50]. They showed that the pore size can be precisely tuned by rapid thermal carbonization in a dilute acetylene atmosphere.

Snyder *et al.* have studied molecular separation behavior by diffusion through the pnc-Si membranes [51]. They performed protein and small molecule separation i and compared the experimental results with theoretical diffusion models. Their experimental results, which showed good agreement with the theory, demonstrated that pnc-Si membranes exhibit little resistance to the diffusion of molecules smaller than the physical pore size cut-off.

Kavalenka *et al.* metallized pnc-Si membranes with gold to use them as flexible conductive electrodes in chemical capacitive vapor sensor [41]. Kavalenka *et al.* also performed detailed studies of gas flow through pnc-Si membranes [57]. Their results demonstrated that changing the pore interior to carbon resulted in flow enhancement. This is due to a change in the nature of molecule–pore wall interactions.

1.3 Objectives and overview of thesis

Although pnc-Si membranes were first reported several years ago, the formation mechanism of the pores is still not understood yet. Since pores are formed in silicon films during crystallization, it indicates that pore formation is thermally driven and is closely related to the phase transition from amorphous to crystalline silicon. This thesis aims to develop a better understanding of the nanopore formation and of how they evolve during annealing. Another objective of this study is to expand the empirical control over the pore characteristics. The goals of this study are:

1. Enriches the fundamental understanding of solid phase crystallization in silicon.
2. Furthers the development of pnc-Si membranes, for example, by exploring new parameters that control the pore properties, including porosity, pore size and pore shape. This will have direct impact in applications such as size-dependent filtration or separation.
3. To explain how the pore formation may be transferred to other materials. We could transfer our understanding to other systems and fabricate porous membranes with materials other than just silicon.

This thesis will systematically study the pore formation process during the solid phase crystallization of silicon films. Chapter 2 will mainly discuss the fabrication process of pnc-Si membrane and characterization methods. Chapter 3 will focus on understanding the effect from the thickness of the capping silicon dioxide films on the pore formation and pore characteristics. In chapter 4, a new capping material, silicon nitride, will be introduced

and incorporated to the three-layer structures. The effect of different capping layer materials on the pore formation will be discussed. Chapter 5 will focus on ex-situ and in-situ annealing study of pore formation in pnc-Si membranes. Finally, in chapter 6 future research directions will be proposed.

Chapter 2 Fabrication and Characterization of Porous Nanocrystalline Silicon Membrane

2.1 Introduction

This chapter focuses on the fabrication and characterization of porous nanocrystalline silicon membrane. The fabrication process involves several steps including photolithography, sputtering, rapid thermal annealing and wet etching. Different techniques can be used to characterize the pnc-Si membrane. These techniques include atomic force microscopy (AFM), scanning electron microscopy (SEM) and transmission electron microscopy (TEM). A customized Matlab script is used to recognize nanopores from TEM images and quantify the pore characteristics including porosity, pore size, pore density and pore distribution.

2.2 Pnc-Si membrane fabrication process overview

Fabrication of pnc-Si membranes involves a strightforward bottom-up approach. First, the backside of a (100) N-type silicon wafer with 100nm thick thermal oxide is patterned using standard photolithography. Then a three-layer stack of SiO_2/a-Si/SiO_2 or Si_3N_4/a-Si/Si_3N_4 is deposited on the front side of the patterned wafer using rf-magnetron sputtering (ATC-2000 V, AJA International, Inc., North Scituate, MA). A rapid thermal processor (RTP) is then used to induce solid phase crystallization (SPC) of the amorphous

silicon layer (Solaris 150, Surface Science Integration, El Mirage, AZ). After annealing the wafer is etched from the patterned side using a customized single-side Si etch cell with a wet anisotropic etchant, ethylene diamine pyrocatechol with pyrazine (EDP-300F, Transene Company, Inc., Danvers, MA) at 110 ℃. The bottom silicon dioxide works as an etch stop because EDP has very high silicon-to-oxide and silicon-to-nitride etch ratios [52]. The protective silicon dioxide films are removed using HF after etching. The whole pnc-Si fabrication process is schematically illustrated in Figure 2-1 and further described in the following subsections.

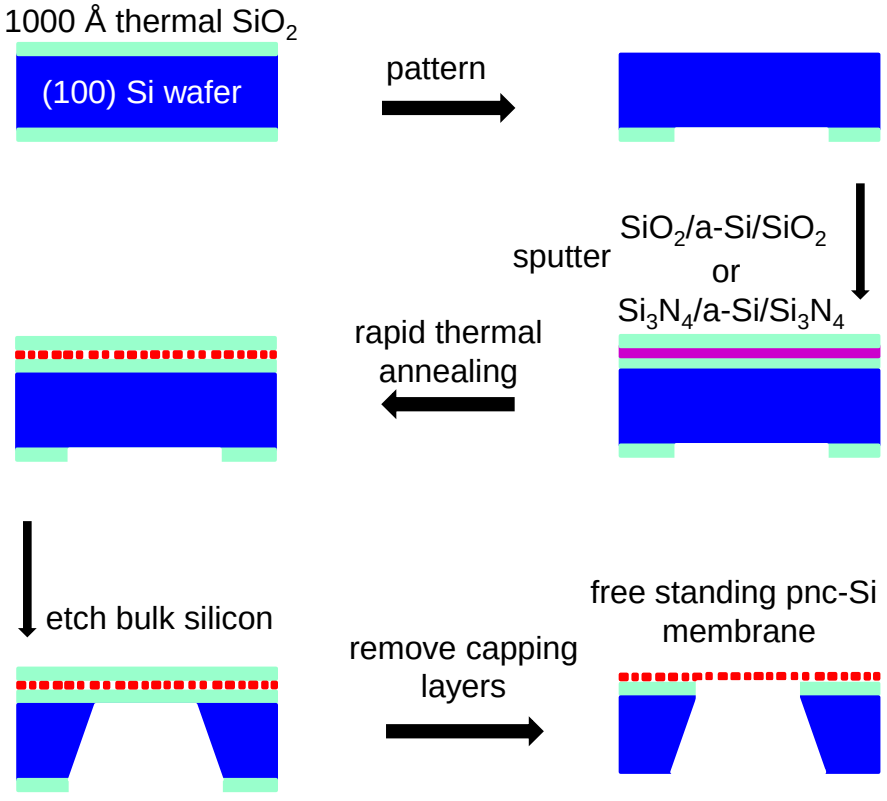


Figure 2-1 Illustration of porous nanocrystalline silicon membrane fabrication process [44, 53].

2.2.1 Photolithography

Photolithography, is a process used in micro fabrication to pattern a thin film or a bulk substrate, such as silicon [54]. This process involves several steps, shown in Figure 2-2. It starts with RCA clean of a bare 4-inch silicon wafer, which is 200μm thick, double side polished N-type with 1~5 Ω·cm and <100> orientation. The RCA clean contains two steps. The first step is standard clean (SC)-1 clean which removes organics and particles. The silicon wafer is soaked in a chemical solution contains deionized (DI) water, aqueous hydrogen peroxide (30% wt H_2O_2) and aqueous ammonium hydroxide (NH_4OH, 29% wt NH_3) with a ratio of 15:5:1 heated at 75℃ for 10 minutes. A brief 20 second dip in 50:1 aqueous hydrofluoric acid (HF) solution is used to remove the native silicon dioxide grown in the RC-1 bath. The second step is RC-2 clean which removes metal contaminants. The RC-2 bath contains deionized (DI) water, aqueous hydrogen peroxide (30% H_2O_2) and hydrochloric acid (HCl, 39% wt) with a ratio of 15:5:1. The silicon wafer is soaked in the RC-2 bath at 75℃ for another 10 minutes and then rinsed and dried.

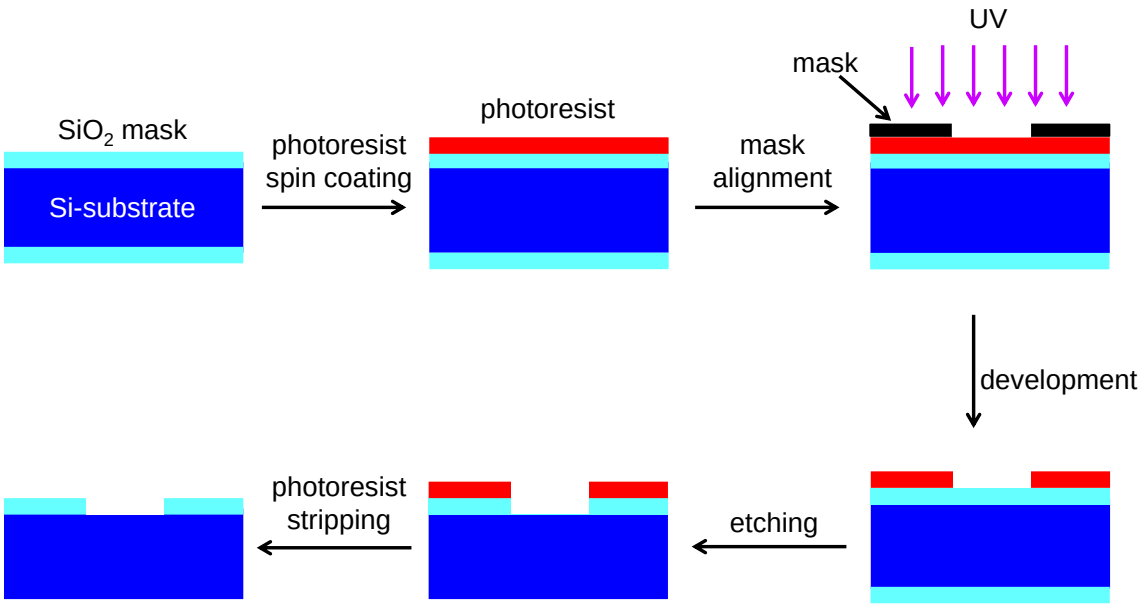


Figure 2-2 Schematic illustration of the photolithography process.

After the RCA clean, 1000Å thick dry thermal oxide films are grown on both side of the silicon wafer in a tube furnace. The dioxide serves as the masking layer and is patterned on the back side of the wafer in the subsequent steps. Hexamethyldisilazane (HDMS) is first spin-coated on the back side of the wafer as the adhesive layer for the photoresist. Approximately 1 μm thick positive photoresist (Shipley 1813) is then spin-coated on the back side of silicon wafer. After a hard bake, the photoresist is exposed to UV light through a patterned photo mask. The pattern is developed and etched into the silicon dioxide with a 10:1 HF solution for 3 minutes 30 seconds. Silicon dioxide film on the front side is also removed in this step. The photoresist is removed in a Piranha solution consisting of a 50:1 mixture of concentrated sulfuric acid (H_2SO_4) and H_2O_2 (30% wt) at 140 ℃ for 10 minutes. The last step for the wafer patterning process is to go through another RCA clean, spinning

and drying sequence of the wafer. Figure 2-3 shows a silicon wafer with a TEM grids pattern.

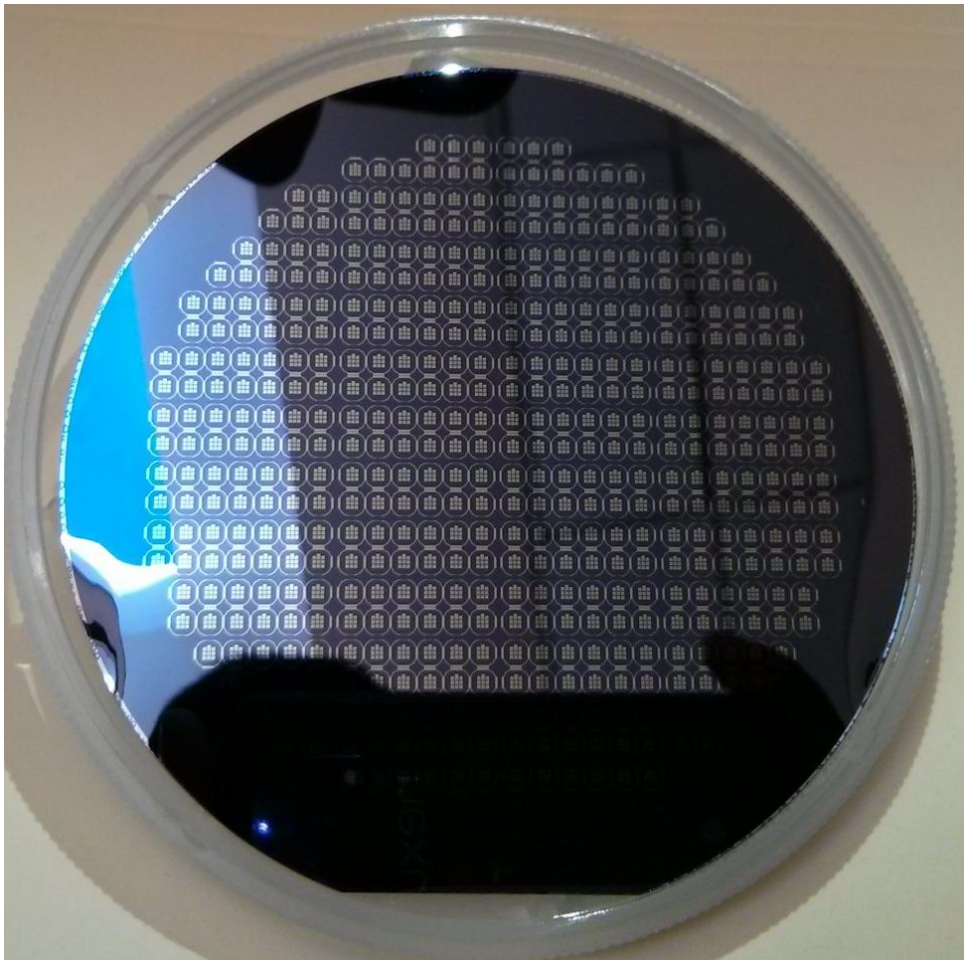


Figure 2-3 Photograph of a silicon wafer patterned with TEM-grid on the back side.

2.2.2 RF Magnetron sputtering

RF magnetron sputtering is a type of physical vapor deposition (PVD), used to deposit thin films of a material onto a surface, known as substrate. A gaseous plasma (usually Ar) is first created between the anode and cathode in a high DC field [55]. Ions

are accelerated, bombard a target, and knock off the target atoms by direct energy transfer. These ejected particles, which can be individual atoms, clusters of atoms, or molecules, travel to the surface of the substrate and form thin films coatings. In RF magnetron sputtering, a magnetron produces strong electric and magnetic fields to confine charged plasma particles close to the surface of sputtered target, which enhances the probability of gas ionization and increases the sputter yield and deposition rate [56]. It is typically used to sputter insulators and semiconductors because this technique prevents charge build-up. Figure 2-4 shows a simplified schematic of rf magnetron sputtering system.

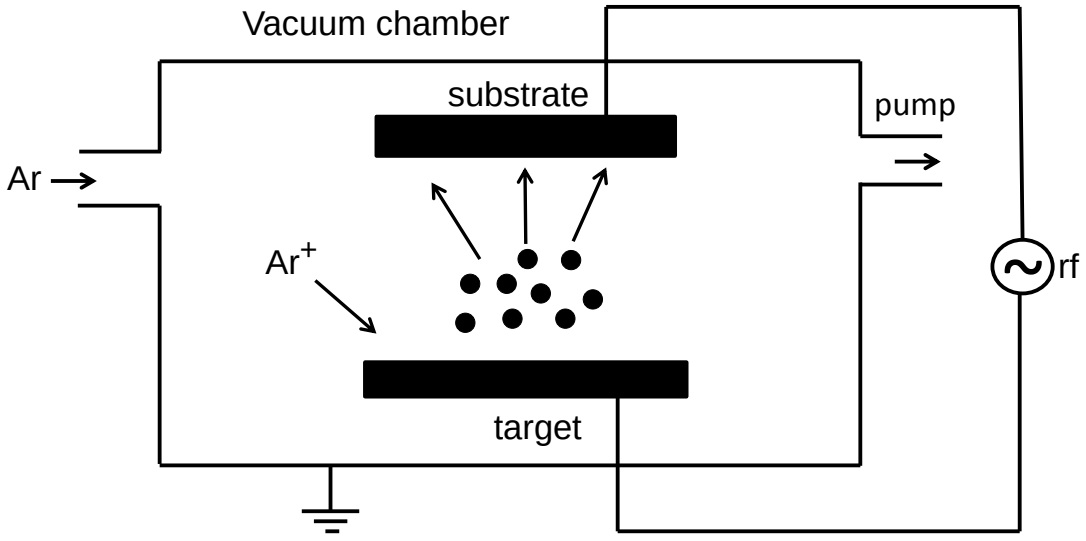


Figure 2-4 Simplified schematic of an rf magnetron sputtering system.

A three-layer structure of SiO_2/a-Si/SiO_2 (short for OSO) or Si_3N_4/a-Si/Si_3N_4 (NSN), is sputtered on the patterned wafer using an AJA International ATC-2000-V RF magnetron sputtering tool (Figure 2-5). In this system, the silicon wafer is placed on a rotational substrate holder with the unpatterned side facing downward to the targets. The substrate

can be heated up to 800 ℃ via tungsten-halogen lamps. The film thickness is determined by the deposition time.

Figure 2-5 Photograph of the AJA International ATC-2000-V RF magnetron sputtering system.

2.2.3 Rapid thermal annealing

The amorphous silicon film are crystallized using rapid thermal annealing (RTA) in the OSO or NSN stack. Pores, which are associated with silicon crystallization, are formed in the silicon film. In RTA, the temperature ramp up rate is very high compared with the furnace annealing. A typical RTA process takes less than 5 minutes.

Our Surface Science Integration Solar 150 rapid thermal process (RTP) shown in figure 2-6, is capable of reaching 1300 ℃ with ramp rates up to 100 ℃/s using 21 tungsten-

halogen lamps arranged above and below a quartz chamber. The silicon wafer sits in a quartz tray with direct contact to a thermocouple underneath. Argon flows into the chamber during the heating process to prevent oxidation of the silicon film. Typical annealing temperature used in the fabrication of the pnc-Si membranes is 1000 ℃, with a 100 ℃/s ramp rate and 1 minute soaking time.

Figure 2-6 Photograph of the Surface Science Integration Solaris 150 rapid thermal processor system.

2.2.4 Silicon wet etching

After the crystallization of the amorphous silicon film in the OSO or NSN stack, the silicon substrate is removed through the patterned windows to release the membrane stack. An anisotropic etchant, Ethylenediamine Pyrocatechol (EDP), is used in the wet etching process. Silicon reacts with EDP to form a compound that is soluble in ethylenediamine. The main reason to use EDP rather than KOH to etch silicon is because that EDP has very

high silicon-to-oxide and silicon-to-nitride etch ratios than KOH. This is also the reason that SiO_2 and Si_3N_4 films can be used as a mask to stop the etching when the silicon substrate is fully removed. EDP etches the silicon (100) plane approximately 20-times faster than the (111) plane. This results the trapezoidal trenches in cross-section after the etching (Figure 2-7).

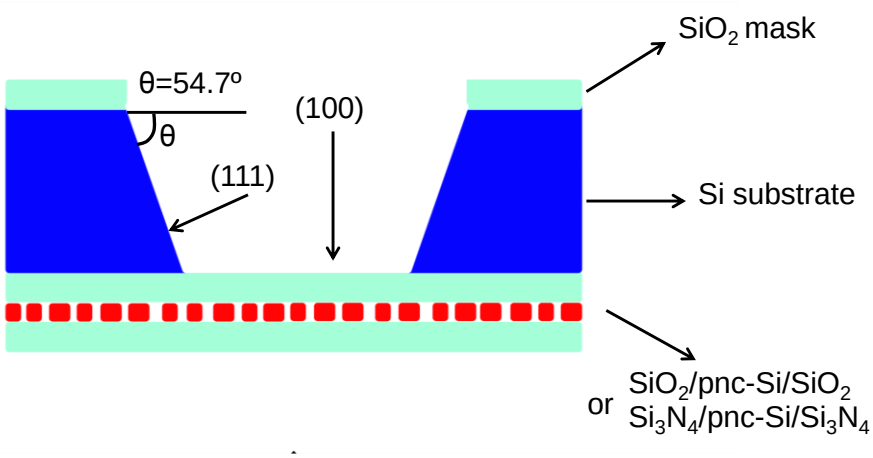


Figure 2-7 Cross-sectional illustration of silicon anisotropic EDP etching.

A customized single silicon wet-etch cell was built by SimPore Inc. for the etching process (Figure 2-8). The wafer is placed inside the etching cell with patterned side up. After it is sealed by the cell body with an O-ring, EDP (Transene, Danvers, MA) is filled in the etch cell and heated to 110 ºC, which gives a etch rate of approximately 1.5μm/min in <100> direction. A magnetic stirrer is used to stir the etchant to keep the etching uniform. Figure 2-9 shows etched free-standing membranes with different geometries.

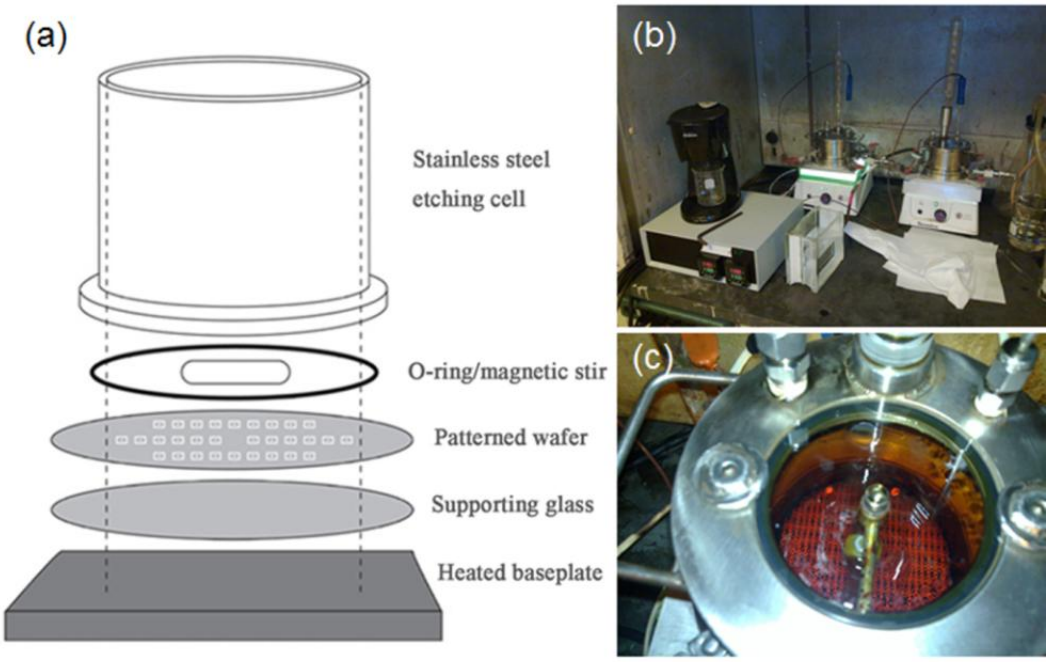


Figure 2-8 (a) Sketch of customized single silicon etch cell, (b) picture of the actual etch cells and (c) top view of patterned wafer toward the end of etching.

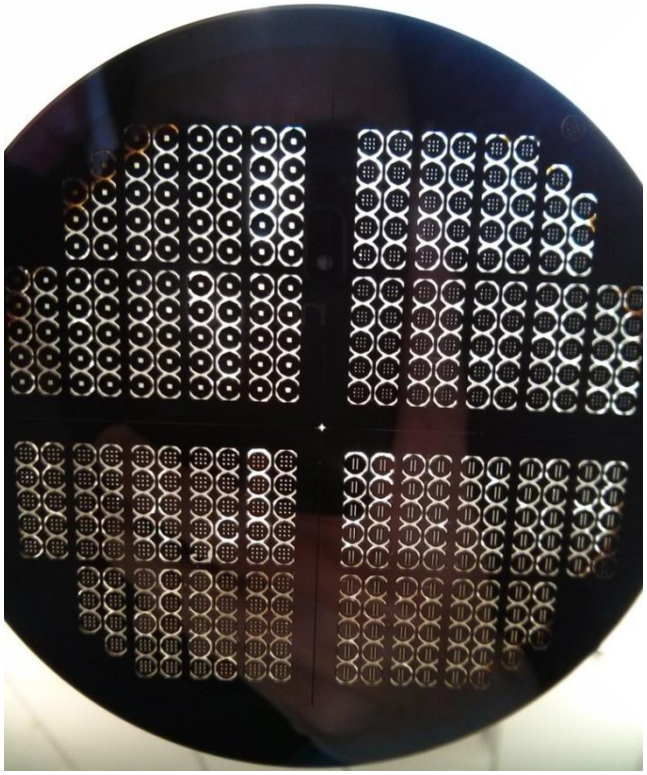


Figure 2-9 Photograph of free-standing pnc-Si membranes with square and slit patterns after removing the silicon substrate. The square and slit features are areas of free-stand pnc-Si membranes.

2.3 Characterization of Pnc-Si membranes

Pores are formed in the silicon film during the silicon crystallization process. Since the diameters of these pores are in nanometer scale, pnc-Si membranes are typically characterized with techniques including atomic force microscopy (AFM), scanning electron microscopy (SEM), and transmission electron microscopy (TEM).

2.3.1 Atomic Force Microscopy

Atomic force microscopy is a very high-resolution type of scanning probe microscopy with a resolution on the order of nanometers or fractions of nanometers scale. It utilizes a cantilever with a sharp tip (probe) at its end to scan the specimen surface and a laser spot that reflected from the top surface of the cantilever is measured into an array of photodiodes when the tip interacts with the sample surface (Figure 2-10). The cantilever is typically silicon or silicon nitride and the radius of the tip is on the order of nanometers.

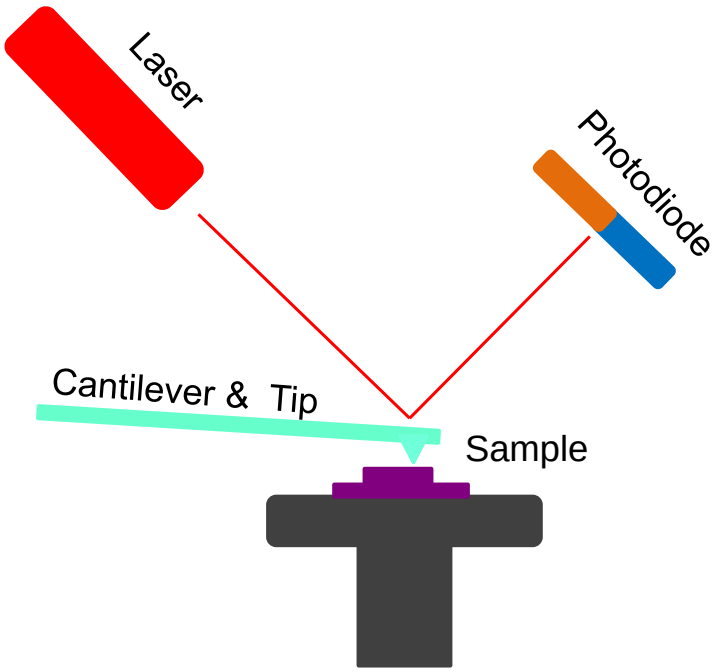


Figure 2-10 Schematic illustration of AFM.

The AFM can be operated in three different modes to image samples, which are contact, non-contact and tapping mode. The contact mode where the tip scans the sample in close contact with the surface is commonly used. Typically the force between the tip and the sample surface is kept constant during scanning process. The drawback of this mode is the potential sample damage and tip broken. In non-contact mode, the tip of cantilever is

oscillated at near-resonance frequency rather than directly contacting with the sample surface. Non-contact mode does not suffer from tip or sample degradation; however, it is affected on samples with adsorbed fluid layers on the surface. Tapping mode, also called semi-contact mode, is similar to non-contact mode, in which the cantilever also oscillates at near-resonance frequency. However, the main difference between tapping mode and non-contact mode is that in tapping mode, the tip of the probe actually touches the sample, and moves completely away from the sample in each oscillation cycle. Tapping mode is now more commonly used to image soft and fragile samples, including membranes. Figure 2-11 is an AFM image of pnc-Si membrane operated in tapping mode.

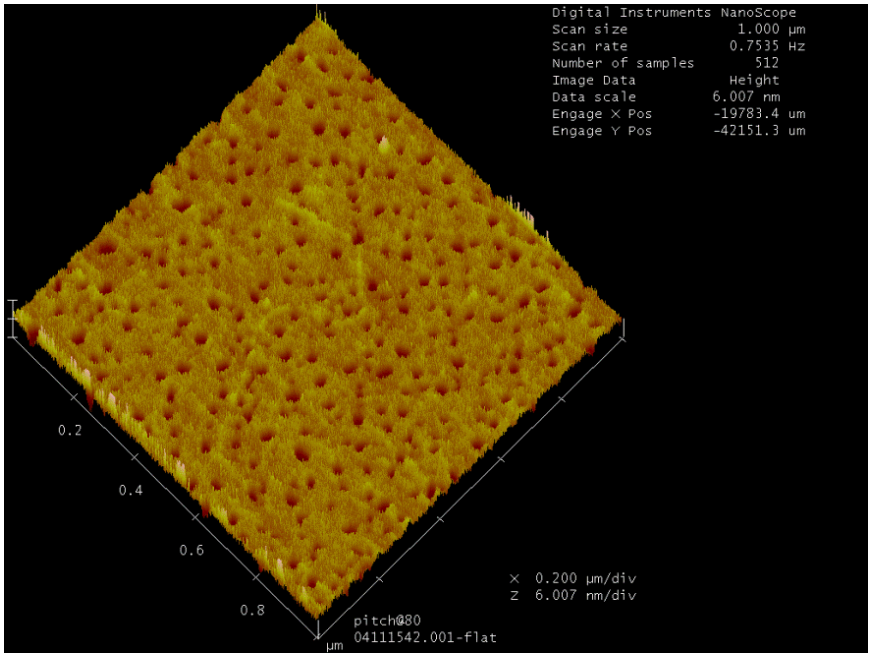


Figure 2-11 AFM image of the pnc-Si membrane.

2.3.2 Scanning electron microscopy

Scanning electron microscopy is a type of electron microscopy that is widely used to image the surface of samples. It scans sample surface with a focused beam of electrons, which interact with sample atoms and produce various signals that can be detected to reveal the surface tomography and compositions.

A Zeiss Supra 40VP SEM is used to image the pnc-Si membrane. Figure 2-12 shows top-down and cross-sectional SEM images of a typical 15 nm thick pnc-Si membrane. In the top-down view, pores appear as the black holes in the crystalline silicon film. The cross-sectional image reveals not only the thickness of the pnc-Si membrane, but also the cylindrical structure of the pore walls [57].

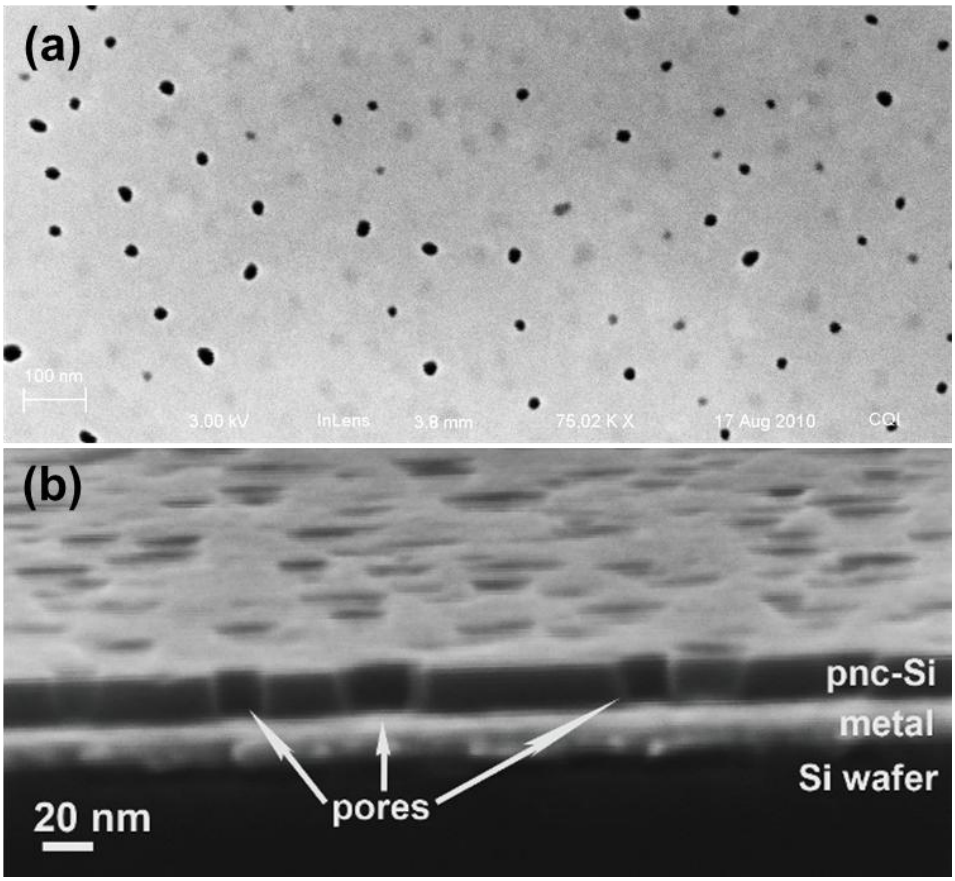


Figure 2-12 SEM images of pnc-Si membrane, (a) top-down view of membrane surface, and (b) cross-sectional view of the membrane [57]. Note: the metal layer is to reduce the charging during imaging.

2.3.3 Transmission electron microscopy

Pore characteristics, including pore size, porosity, pore shape, pore density and pore distribution, are of great interest for most porous membranes. Because of the ultra-thin nature of the pnc-Si membrane, transmission electron microscopy (TEM) can be directly used to characterize the nano-size pores without any time-consuming sample preparation process. In the TEM image (Figure 2-13), nanopores appear to be white spots since the electron beam passes through pores collinearly without any interactions and hence shows bright spots. On the contrary, silicon nanocrystals appear show the gray or black contrast in the TEM image, which is due to the diffraction of silicon nanocrystals with different orientations.

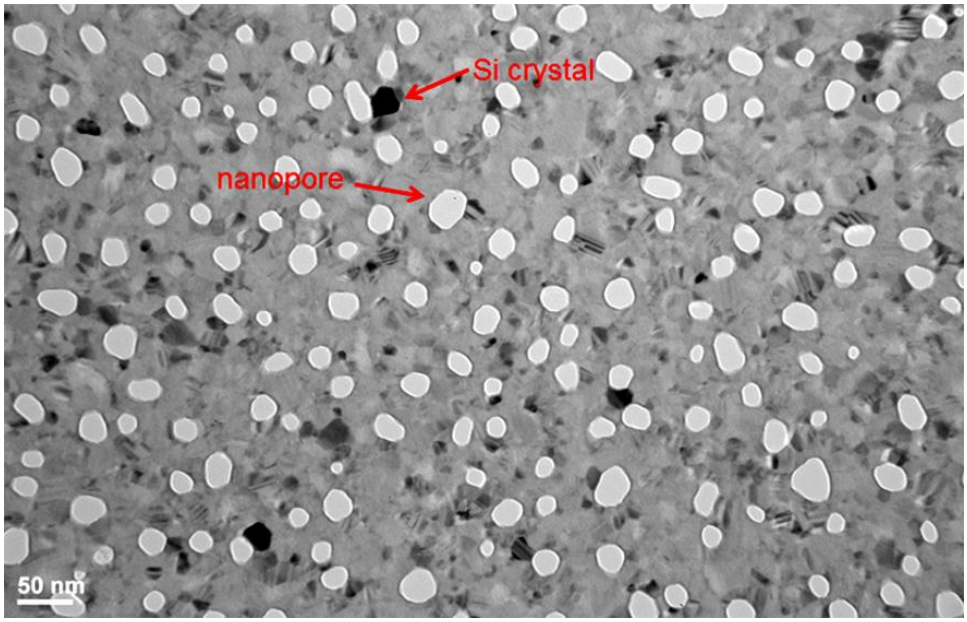


Figure 2-13 Bight field TEM image of the pnc-Si membrane. The white spots represent nanopores where the black regions denote silicon nanocrystals

A customized image processing program written in MATLAB (available at http://nanomembranes.org/resources/software/) is deployed to analyze the pore characteristics of the pnc-Si membrane TEM images (Figure 2-14). The TEM image is first processed with a background correction by subtracting the average value from a local region of defined size from each pixel. Then the image is transformed into a black and white binary image using a threshold value. The rule in selecting this threshold value is that most pore pixels should have an intensity value that is higher than the threshold value while the background pixel should mostly fall below. In the new binary image values higher than the threshold are white and those below the threshold are black. Combinates of binary operations are then used to remove artifacts and recognize pores more precisely in the image. After that pore edges are identified in the TEM image and pore characteristics,

including diameter, pore area, and porosity, are found. For a non-circular pore, the equivalent dimater is defined as the diameter of a circle that has the same area as that of the non-circular pore. This equivalent diameter also applies to pores in the edge. Lastly pore distributions are typically found by plotting the pore density at each pore diameter. Average diameter and porosity are indicated above the plot. In order to verify the validity of the resulted pore characteristics from the TEM image of single position, different locations of the pnc-Si membrane have been imaged. The standard error for the porosity value and average pore diameter from different locations of the same membrane is low, so statistics from any random location of the membrane can be assumed to represent values for the whole membrane [58].

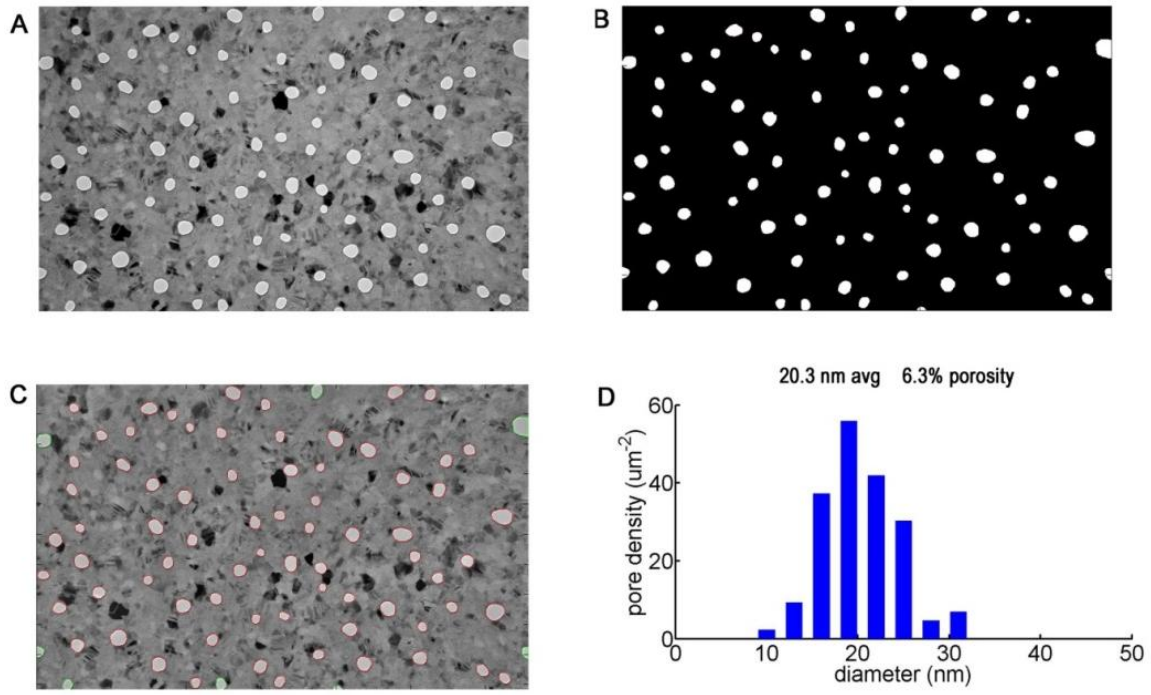


Figure 2-14 Pore recognizing process of pnc-Si membrane TEM image.

2.4 Conclusion

In this chapter, the fabrication and characterization of pnc-Si membrane is briefly discussed. The fabrication process is straightforward, which starts with patterning of silicon wafer, follows with sputtering, rapid thermal annealing and finishes by silicon substrate wet etching. Pores are spontaneous formed during the solid phase crystallization of the silicon film and are the order of nanometers scale in diameter. They can be characterized using AFM, SEM and TEM.

Chapter 3 Effect from Silicon Dioxide Capping Layers on Pore Formation

3.1 Introduction

In this chapter, the effect of oxide capping layers on the pore formation process in pnc-Si membranes is studied. Both the top and bottom oxide layers with different thickness have been tested on silicon dioxide/ silicon/ silicon dioxide (OSO) stacks. Pore characteristics including pore size, porosity, and pore distribution are compared and summarized. The effect from both the top and bottom capping layers on pore formation is further discussed.

3.2 Oxide Capping Layers Effect on Pore Formation

Ultrathin porous nanocrystalline silicon (pnc-Si) membranes fabricated by crystallizing amorphous silicon thin films were first published by Striemer et al. [44] in 2007. Nano-sized pores are formed in a sputtered silicon film sandwiched by two silicon dioxide films during the solid state crystallization process. Since the discovery of the pnc-Si membrane, a lot of research [39-43, 49-51, 57] has been carried out to develop and utilize this novel membrane material. Fang et. al. [43] reported several parameters to control the pore properties. These parameters include annealing temperature, ramping up

rate and silicon film thickness. However, the mechanism for pore formation in pnc-Si membrane remains poorly understood.

It has been observed that pore formation is always associated with the solid-phase crystallization of silicon film during the annealing process. In this three-layer structure, silicon film is sandwiched by two silicon dioxide films during the crystallization. Researchers have shown that SiO_2 capping layer affects the silicon crystallization by acting as either a heat reservoir or a heat sink depending on its thickness [59-61]. Limited research has been done to investigate the effect of the capping layers on the pore formation, which might give insight into the mechanism of pore formation.

To systematic investigate the effects from the capping oxide layers on pore formation, experiments are conducted onto top and bottom oxide sections. The amorphous silicon layers are kept at 15nm in all stacks while the silicon dioxide capping layers are made with different thicknesses. In the top oxide study, the thickness of the top oxide is varied from 1nm to 5nm, 10nm, 20nm, 40nm, and up to 100nm respectively while the bottom oxide layers keep at 20nm. In the bottom oxide study, the thickness of the bottom oxide is varied from 5nm to 20nm, 40nm, and up to 100nm respectively while the top oxide layers are kept at 20nm. All thicknesses are calibrated by spectroscopic ellipsometer (VASE, J. A. Woollam Co., Inc., Lincoln, NE). Samples are all rapidly thermal annealed at 1000 ℃ with a 100 ℃/s ramp rate and a soaking time of 1 minute at 1000 ℃.

3.2.1 Effect from the top oxide layer

OSO stacks with different thick top oxide layers are annealed at 1000 ℃ to introduce solid phase crystallization and pore formation in silicon films. Table 3-1 shows the geometry details of these samples. After annealing these samples are characterized with transmission electron microscope.

Table 3-1 Geometry thickness of the OSO stacks in the top oxide section.

Sample number	Top oxide layer thickness (nm)	Amorphous silicon thickness (nm)	Bottom oxide layer thickness (nm)
1	1	↑	↑
2	5	↑	↑
3	10	15	20
4	20	↓	↓
5	40	↓	↓
6	100	↓	↓

Figure 3-1 shows TEM images of annealed 15nm thick pnc-Si membranes with different thick top oxide layers. TEM images clearly show that only a few pores are formed in sample with 1nm top oxide layer. Both the pore size and pore density increase significantly as the top oxide layer increases from 1nm to 5nm and then seem to saturate as the top oxide layer goes thicker.

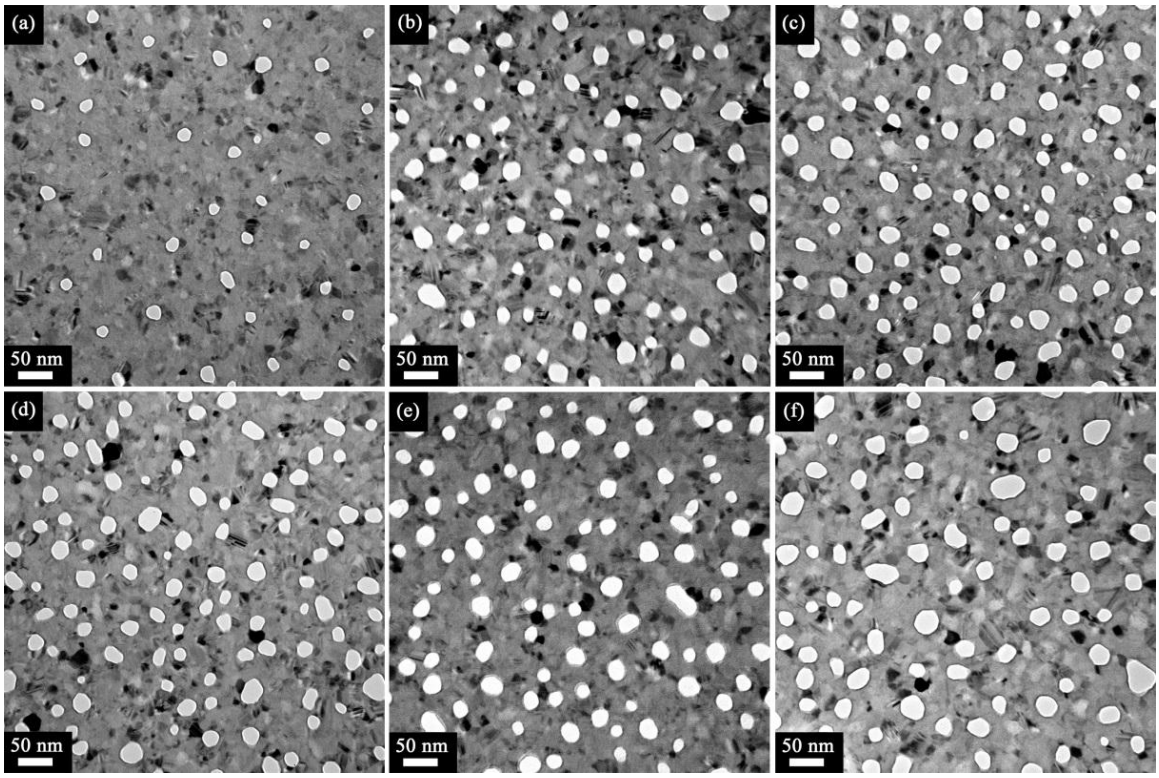


Figure 3-1 TEM images of annealed 15nm thick pnc-Si membranes with 20nm bottom oxide and different thick top oxide layers ranging from (a) 1nm, (b) 5nm, (c) 10nm, (d) 20nm, (e) 40nm, and (f) 100nm.

The pore characteristic plots (figure 3-2) quantitatively confirm the trend of pore growth with the top oxide layers observed from TEM images. The porosity increases rapidly from 2.9% to 10.5% as the top oxide goes from 1nm to 5nm. Then it quickly reaches to saturation at around 12.5% when the top oxide passes 10nm. The highest porosity is 13.1% from sample with 100nm top oxide. The APD plot shows a very similar trend as to the porosity plot. It starts at 16nm from 1nm top oxide sample, quickly increases to 22.5nm as the top oxide increases to 5nm and stabilizes at around 22.5nm with the increase of the top oxide. Sample with 100nm top oxide produces the highest APD of 24.3nm. Pore

distribution plot clearly reveals the distribution difference between sample with 1nm top oxide and the rests. Majority pores are from 13nm to 19nm in diameter in the 1nm top oxide sample. With the increase of top oxide thickness, the size of majority pores quickly shifts to larger diameters from 19nm to 27nm for the other samples.

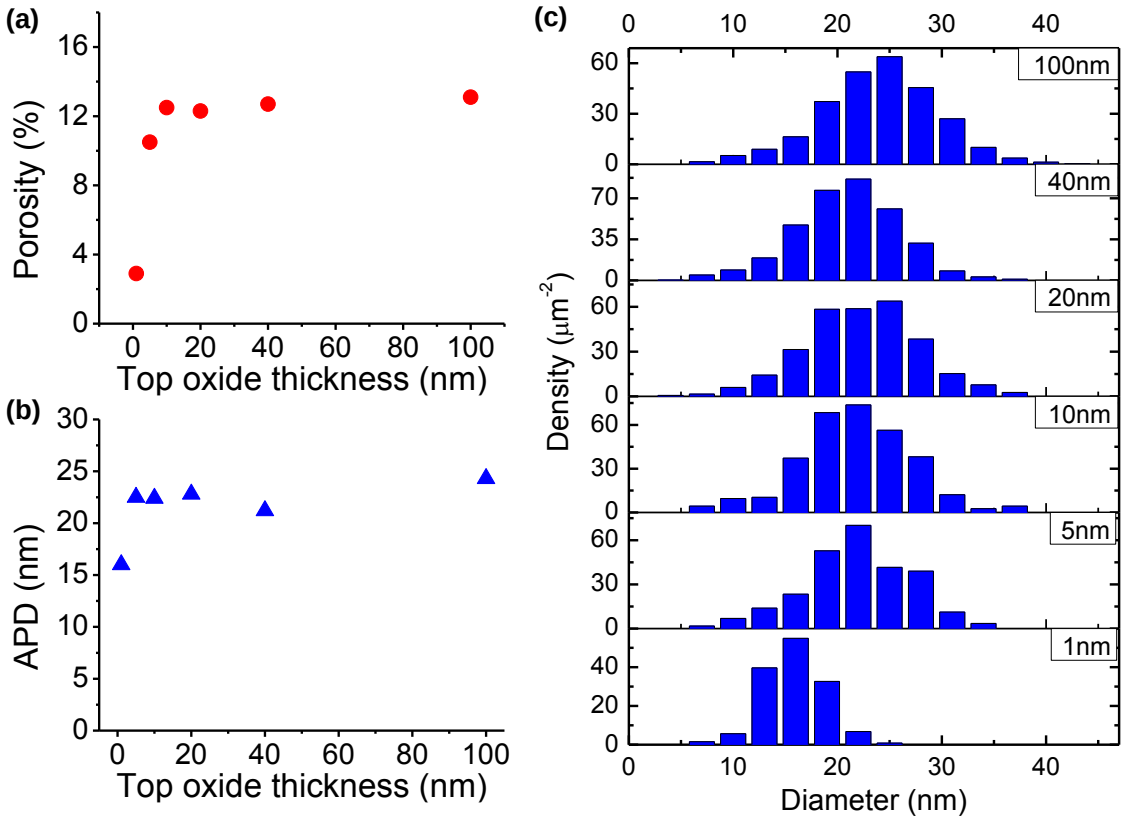


Figure 3-2 Pore characteristics plots of annealed samples with different thick top oxide layers, (a) porosity, (b) APD and (c) pore size distribution.

The pore characteristics comparisons show that sample with 1nm top oxide produces the least and smallest pores in all samples. Both the porosity and pore size increase rapidly as the top oxide layer becomes thicker. However, pore formation is less affected once the

top oxide film passes 10 nm thick. This indicates that pore formation is very sensitive a very thin top oxide film.

To further investigate this effect, a two-layer structure of an amorphous silicon film of 15nm on a 20nm bottom silicon dioxide layer has been tested. It can be recognized as a 0 nm top oxide sample. This sample is annealed at the exact same condition. Figure 3-3 shows the scanning electron microscopy (SEM) images of this sample after the rapid thermal annealing. Interestingly, three-dimensional silicon crystalline islands, instead of nanoporous silicon film are formed after annealing. Some of these agglomerated islands are spherical or rodlike and some are irregular. The size of these islands is from several tens to a few hundred nanometers in diameter and the height is around 100nm. It tells that silicon crystallization is accompanied by the well-known process of agglomeration when no top oxide is present.[62-67] The agglomeration of silicon films during crystallization is due to the strain energy and surface energy.[64, 67]

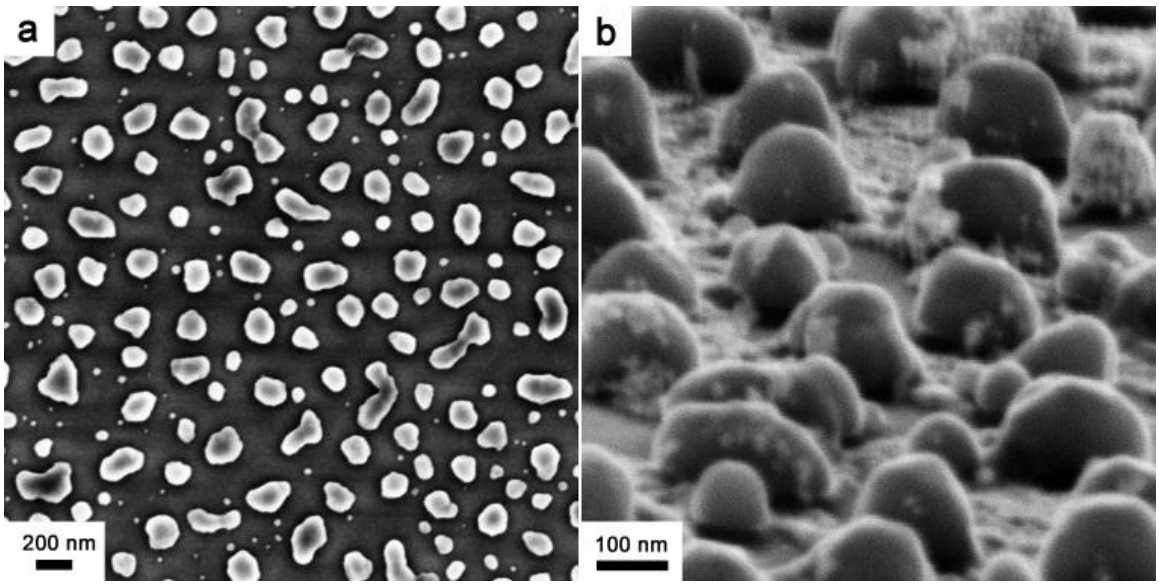


Figure 3-3 SEM images of non-top oxide sample after annealing, (a) top-down view, and (b) cross-sectional view.

This result shows a transition from nanopore formation to silicon islands agglomeration as the top oxide layer decreases from 1 nm to 0 nm. It indicates that the top oxide film is essential for the pore formation, which provides confinement on silicon film to prevent it from surface-energy-driven agglomeration [64, 67].

3.2.2 Effect from the bottom oxide layer

Bottom silicon dioxide layer is quite important in the pore formation process. It works not only as the etching stop in fabrication process, but also as a barrier layer between the amorphous silicon film and silicon substrate to prevent homo-epitaxy [68-71] of the amorphous silicon in the solid phase crystallization. So the bottom oxide layer is also essential in the pore formation process.

Table 3-2 Geometry thickness of the OSO stacks in the bottom oxide section.

Sample number	Bottom oxide layer thickness (nm)	Amorphous silicon thickness (nm)	Top oxide layer thickness (nm)
1	5	↑	↑
2	10	↑	↑
3	20	15	20
4	40	↓	↓
5	100	↓	↓

Bottom oxide layers with four different thicknesses ranging from 5nm, 10nm, 20nm, 40nm and 100nm have been tested in OSO stacks (table 3-2). Figure 3-4 shows the TEM images of annealed pnc-Si membranes with different thick bottom oxide layers. Interestingly, by directly comparing TEM images, bottom oxide layer shows an opposite effect on pore formation as to the top oxide. Pore size and density does not change very much when the bottom oxide layer increases from 5nm to 40nm. However, a sharp decrease in both pore size and density show up in sample with 100nm bottom oxide layer.

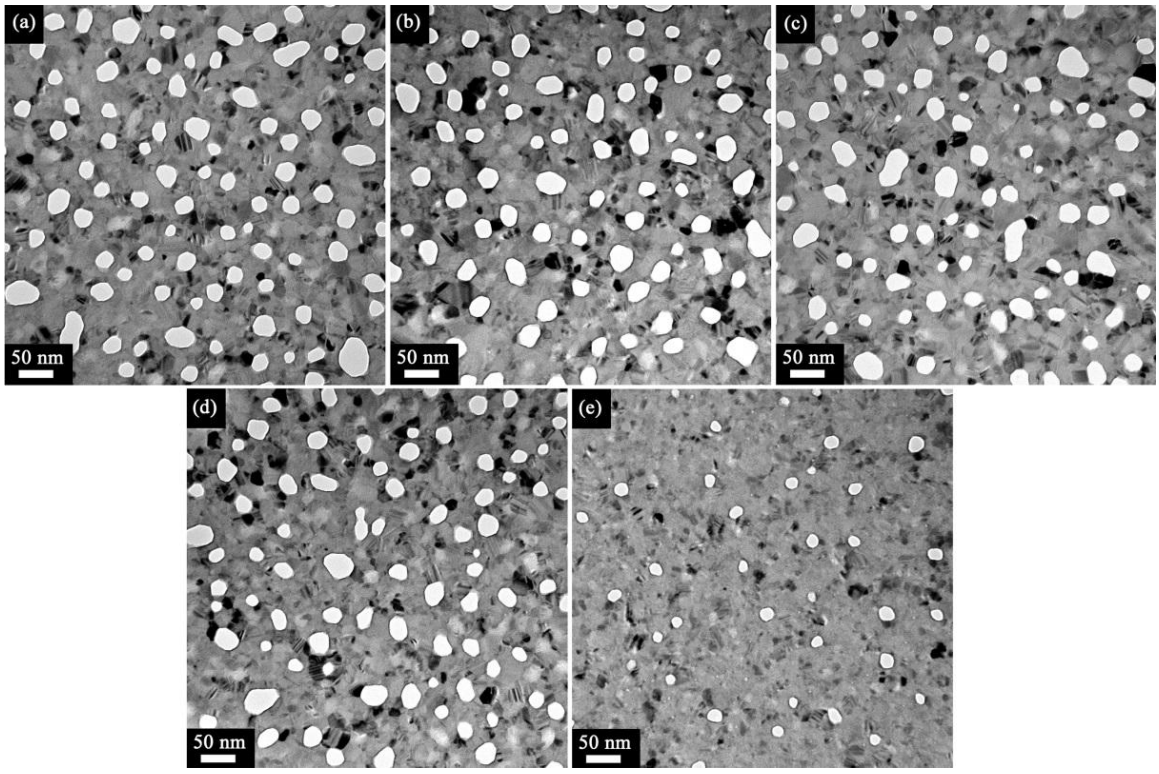


Figure 3-4 Pnc-Si membranes annealed at 1000 ℃ with different thick bottom oxide layers (a) 5nm, (b) 10nm, (c) 20nm, (d) 40nm and (e) 100nm.

The pore characteristic plots in figure 3-5 clearly confirm this trend. The porosity is 14.5% from sample with 5nm bottom oxide, decreases a little to 12.6% when the bottom oxide layer increases to 40nm, and dramaticly drops to 2.5% as the bottom oxide layer increases to 100nm. The APD plot shows a similar trend that it does not change very much as the bottom oxide layer increases from 5nm to 40nm. However, the APD decreases from 24nm to 15nm as the bottom oxide increases from 40nm to 100nm. The pore size distribution plot clearly reveals that the majority pores of the sample with 100nm bottom oxide shifts to smaller size with lower pore density, which is in consistent with the porosity and APD results.

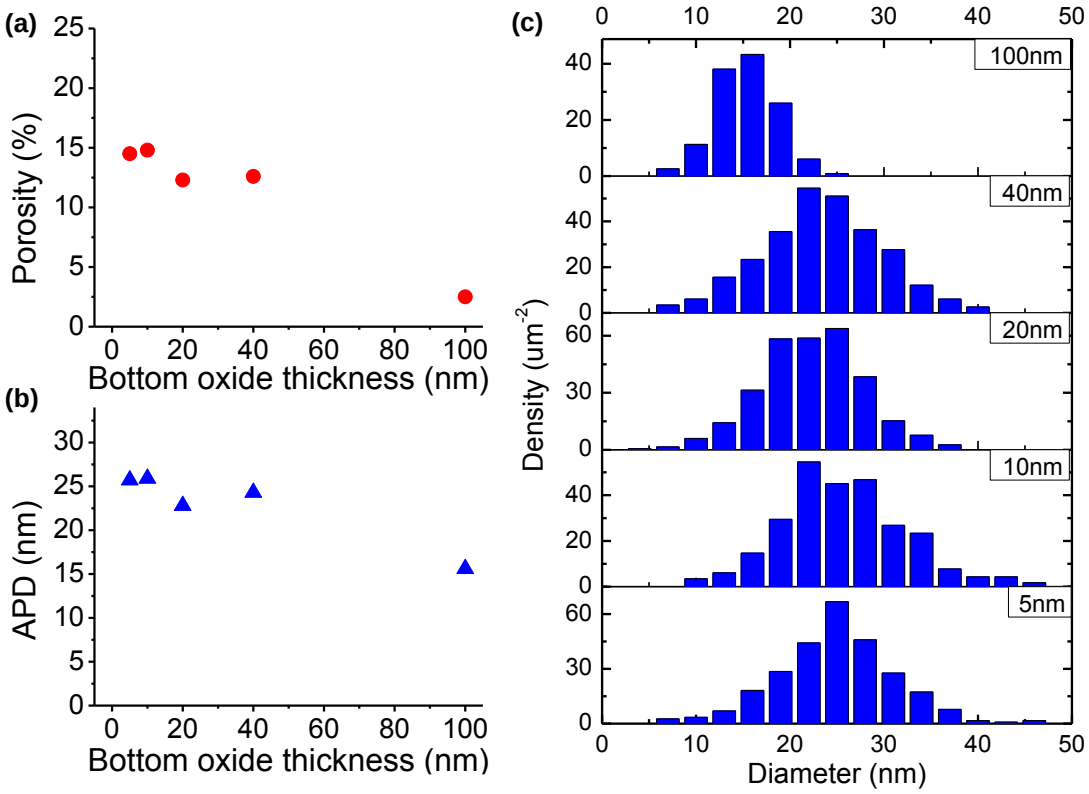


Figure 3-5 Pore characteristics plots of annealed samples with different thick top oxide layers, (a) porosity, (b) APD and (c) pore size distribution.

The pore characteristic results indicate that the pore formation is less affected as the bottom oxide layer increases from 1nm to 40nm. However as the bottom oxide layer goes thicker, pore formation starts to be strongly affected. Both the porosity and APD drops dramatically as the bottom oxide layer increases to 100nm, which demonstrates that thicker bottom oxide layer shows a strong inhibitation effect on pore formation.

Since the pore formation is associated with the silicon crystallization, it is possible that silicon crystallization process is affected as the bottom oxide becomes thicker. It has been reported that the surface roughness strongly affects the nucleation mechanism in solid-phase crystallization of amorphous silicon films.[72, 73] A Rough interface might decrease the diffusivity of silicon atoms and hinder nanocrystal nucleation,[72] which would suppress pore formation.

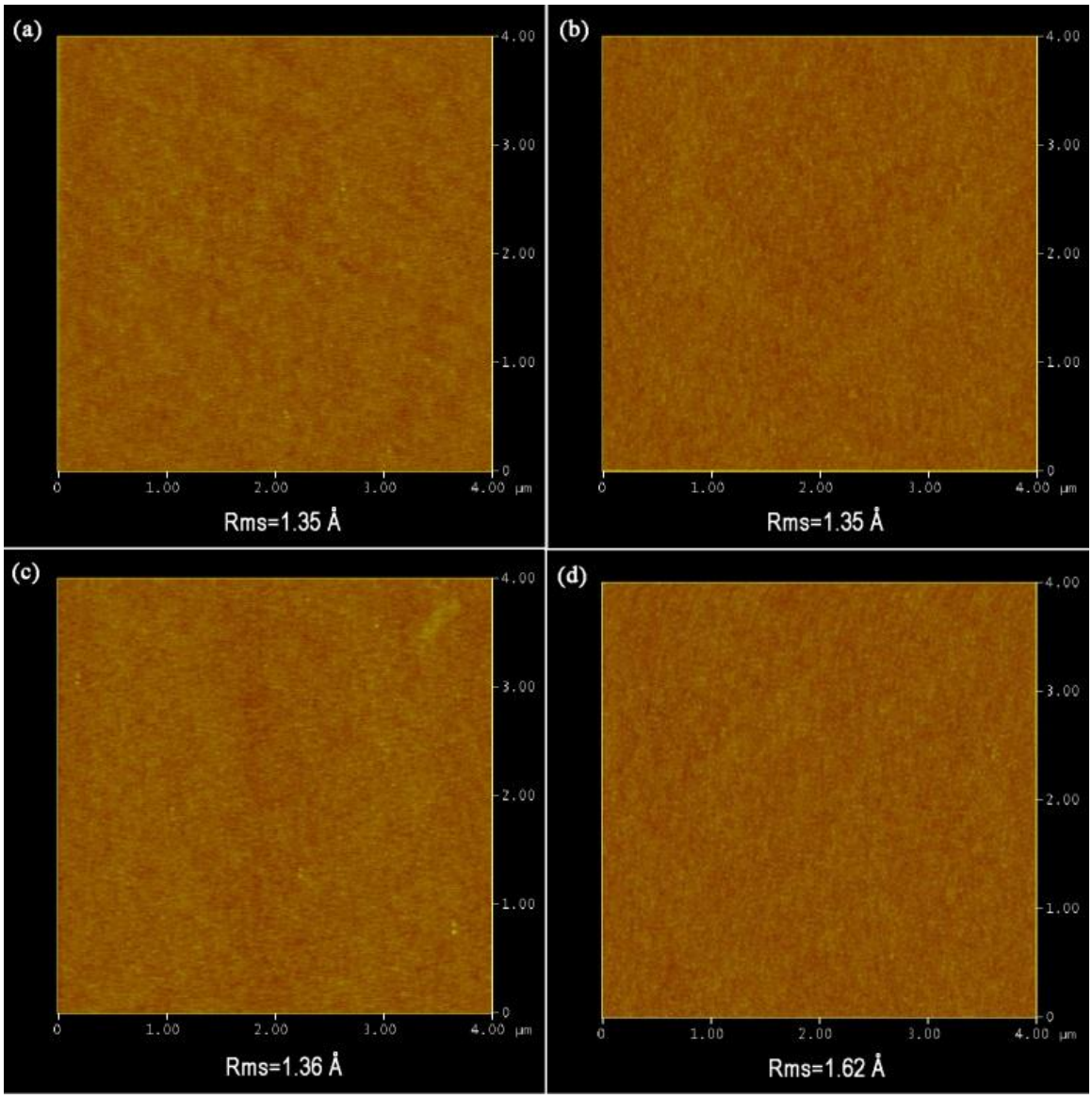


Figure 3-6 AFM images of SiO2 films with different thicknesses, (a) 5nm, (b) 20nm, (c) 40nm and (d) 100nm.

Atomic force microscopy (AFM) is deployed to measure the roughness of silicon dioxide films deposited on silicon substrates with four different thicknesses from 5nm, to 20nm, 40nm and 100nm. Figure 3-6 shows the AFM images of silicon dioxide films. Root

mean square (RMS) roughness is considered as it is scan length dependent. The roughness result shows that 5nm, 20nm and 40nm SiO2 layers have very close RMS roughness of 1.35 Å. The RMS roughness of 100nm SiO2 film increases to 1.62 Å. This result supports the claim that a rough interface will suppress nanocrystal nucleation and thus severely limit pore formation. TEM images also confirm that the sample with 100nm bottom oxide layer yields smaller nanocrystals than other samples. This result shows that interface roughness is very important during pore formation process as it directly affects the silicon crystallization.

3.3 Conclusion

In this chapter, we have demonstrated that both the top and bottom silicon dioxide films are essential to the pore formation process in pnc-Si membranes. Silicon crystallization is accompanied by the process of agglomeration when no top oxide layer is present. The pore size and porosity increase rapidly as the thickness of the top oxide layer increases and quickly reach to saturation when the top oxide passes 10nm. The bottom oxide, on the other hand, works as a barrier layer to prevent the homo-epitaxy of silicon films during rapid thermal annealing process. The pore size and porosity decrease as the thickness of the bottom oxide layer increases. This can be explained by the roughness increasing with bottom oxide thickness since rough interface hinders nanocrystal nucleation which subsequently limits nanopore formation. It also indicates that interface roughness in the three-layer stack is an important factor to affect the pore formation process in pnc-Si membrane.

Chapter 4 Effect from Capping Layer Materials on Pore Formation

4.1 Introduction

This chapter focuses on studying the effect of capping layer materials on pore formation process in pnc-Si membranes. Silicon nitride is introduced to replace the silicon dioxide layers in the three-layer structure. Four different thin film stacks including silicon nitride/silicon/silicon nitride (NSN), silicon dioxide/silicon/silicon nitride (OSN), silicon nitride/silicon/silicon dioxide (NSO), and silicon dioxide/silicon/silicon dioxide (OSO) are annealed under different temperatures. Pore characteristics from these four stacks are compared and discussed. The NSN stacks with different thick silicon films are particular investigated.

4.2 Capping Layer Materials Effect

In chapter 3 we have shown that one of the prerequisites for the nanopore formation in the silicon film is the presence of both the top and bottom SiO_2 layers.[74] The top SiO_2 layer prevents the silicon film from agglomerating [75] while the bottom SiO_2 layer works as a barrier layer to prevent homoepitaxy [76, 77] during annealing. Recent results by Balachandra Achar et al. [78] confirm our results even though their deposition technique was different and they used much thicker SiO_2 layers. Experimenting with barrier layers

other than silicon dioxide could be a first step toward generalizing the phenomenon to other material pairs. Silicon nitride, another dielectric material with favorable optical properties, high thermal stability, chemical inertness, and good dielectric properties, has been widely used in optoelectronic devices [79, 80] and integrated circuit fabrication processes such as gate dielectrics, diffusion barriers, isolation materials and final passivation layers.[81-83]

Table 4-1 Geometry details of four stacks.

Stack structure	Si layer (nm)	Si3N4 layer (nm)	SiO2 layer (nm)
NSN	25	30	-
NSO	25	30	-
OSN	25	30	30
OSO	25	-	30

We incorporate silicon nitride as an alternative barrier layer in stack geometry. To systematically study the effect from this new capping layer, three new stacks NSN, NSO and OSN, combined with the OSO stack as control sample are tested and discussed. The difference between the NSO and OSN stacks is the deposition order. The NSO stack starts the deposition with silicon nitride layer and ends with the oxide layer where the OSN stack is the opposite deposition order. Table 4-1 shows the geometry details of each stack. These samples are annealed at four different temperatures including 800 ℃, 900 ℃, 1000 ℃ and 1100 ℃ . We did not explore higher annealing temperatures because delamination of the films was observed after annealing at 1200 ℃. The annealing process involves a fast ramp rate of 50 ℃/s and a soaking time of 1 minute at each set temperature.

4.2.1 Pore Formation in the NSN Stack

The crystallization of silicon film sandwiched by nitride layers is associated with pore formation. Figure 4-1 shows TEM images RTP annealed NSN stacks at different temperatures, which clearly shows the pore formation in silicon films. This is the first time that pores are reported in ultrathin Si membranes fabricated using another system besides the OSO system.

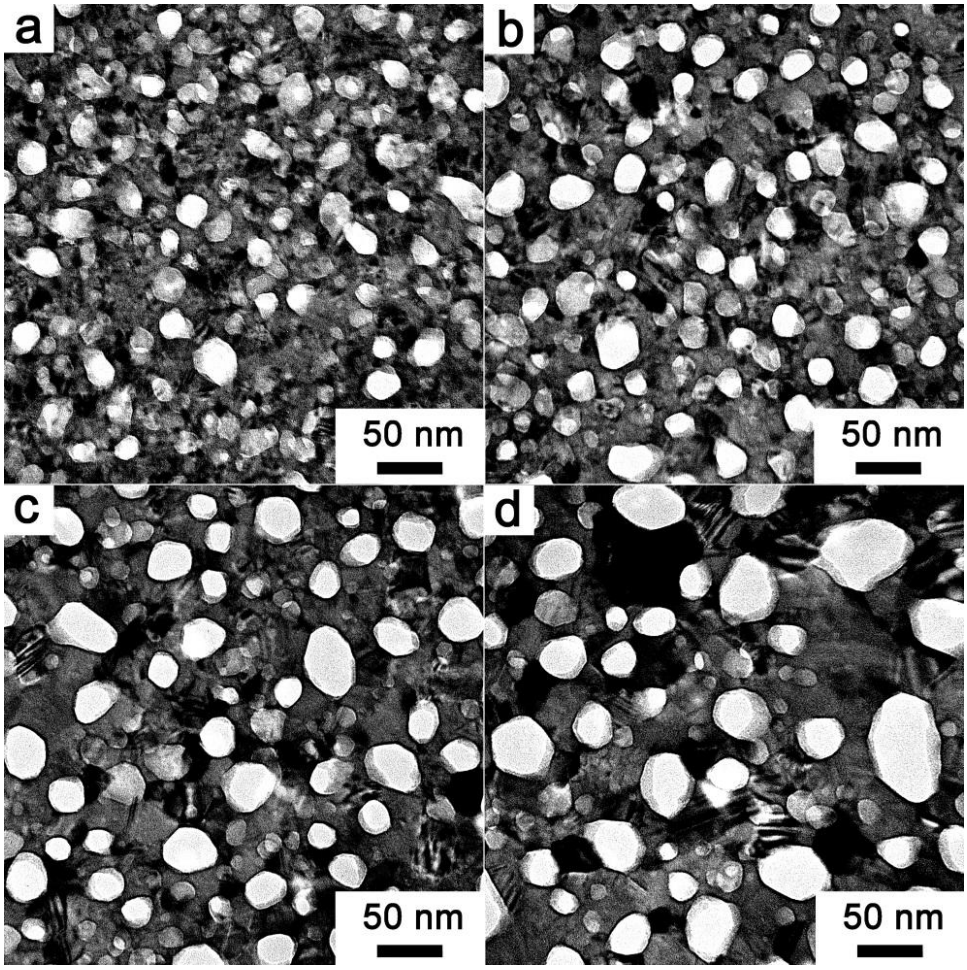


Figure 4-1 TEM images of the NSN system after RTP annealing at a) 800 ℃, b) 900 ℃, c) 1000 ℃ and d) 1100 ℃.

It can be clearly seen that nanopores are formed in the NSN samples at all annealing temperatures. With the increase of annealing temperature, both the sizes of silicon crystals and pores are growing bigger. The pore characteristic plots in figure 4-2 support the trend of pore growth with the annealing temperatures observed from TEM images. The porosity increases rapidly from 4% to 19% as the annealing temperature goes from 800 ℃ to 1100 ℃. The APD plot shows a very similar trend. It starts at 16nm at 800 ℃, quickly increases to 24.5nm as the annealing temperature increases to 1000 ℃ and stops at around 26nm at 1100 ℃. Pore distribution plot clearly reveals that both the pore number and pore size increase with the annealing temperature, which is consistent with our previous results.

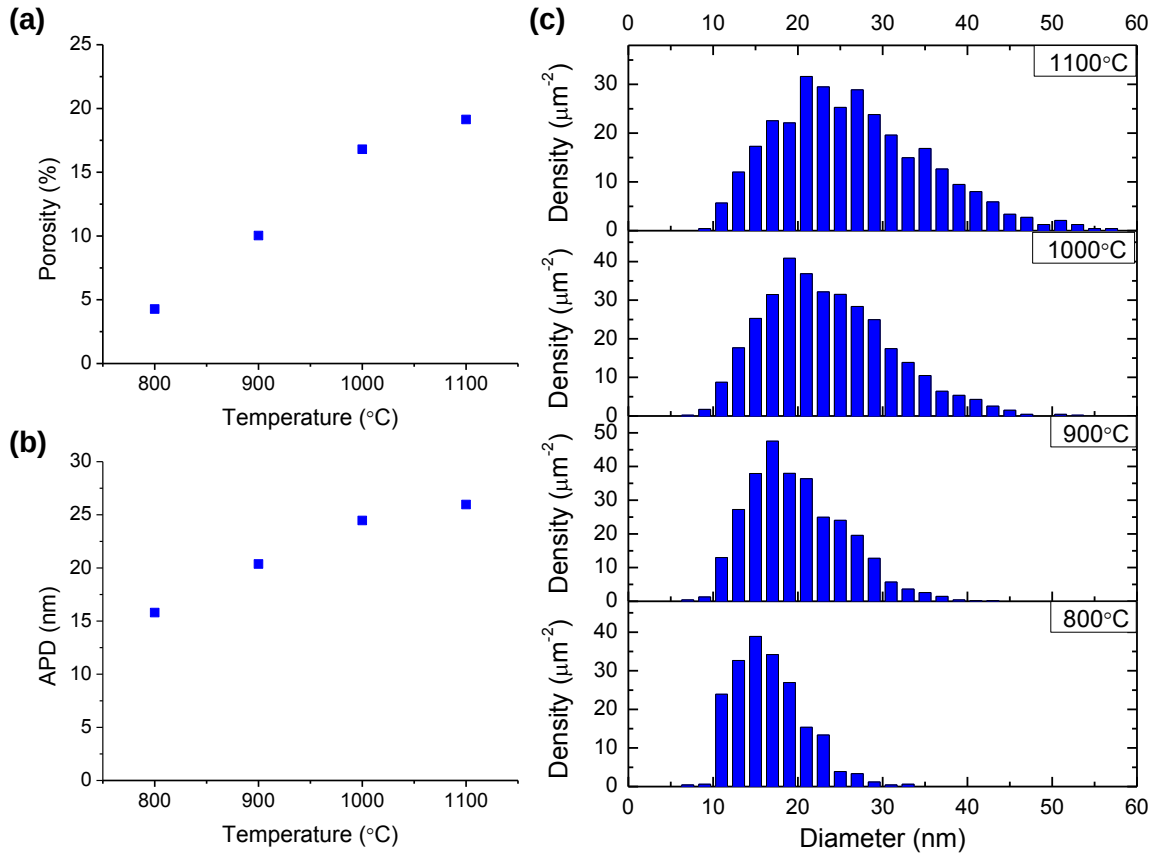


Figure 4-2 Pore characteristic plots of the NSN system after RTP annealing, a) porosity, b) APD and c) pore size distribution.

4.2.2 Pore Formation in the NSO Stack

Since nanopores can be formed in both the NSN and OSO systems, it is likely that nanopores would be formed in the mixed NSO and OSN systems. Figure 4-3 shows TEM images of the NSO stacks annealed at four different temperatures. Nanopores are formed in silicon films, as we expected.

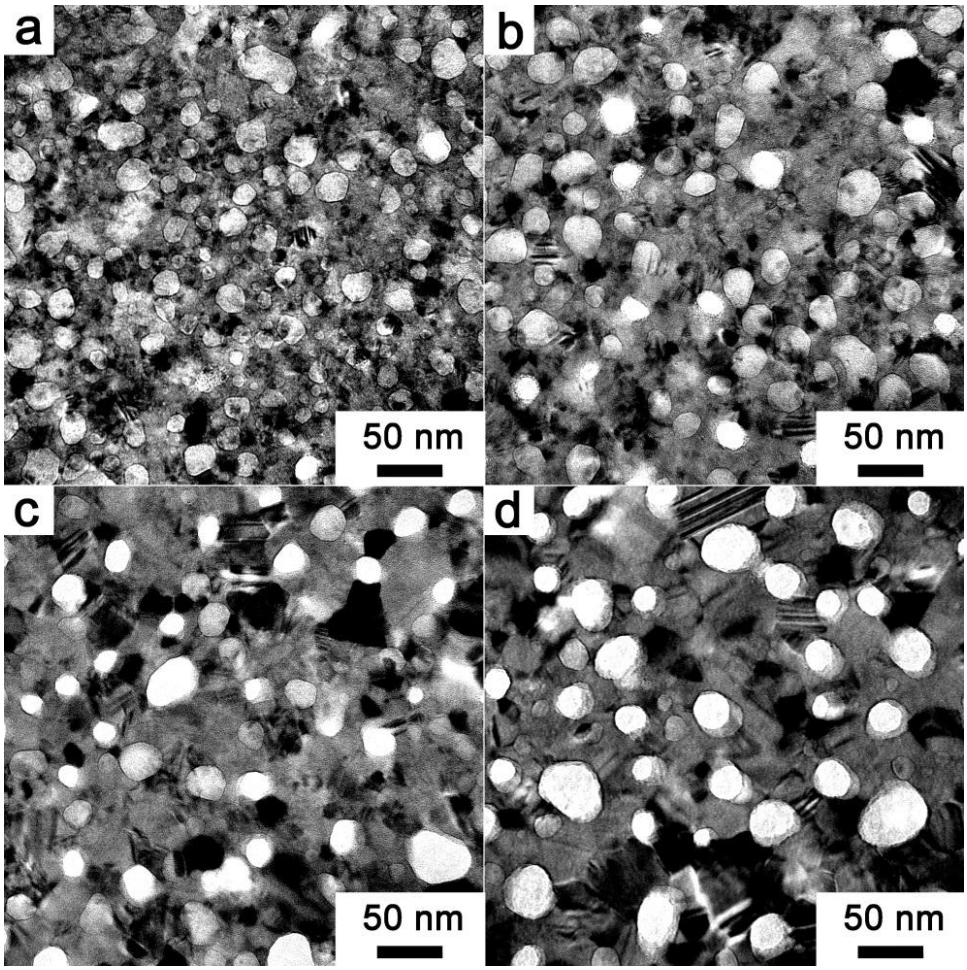


Figure 4-3 TEM images of the NSO system after RTP annealing at a) 800 ℃, b) 900 ℃, c) 1000 ℃ and d) 1100 ℃.

The pore characteristic plots of the NSO system in figure 4-4 shows a similar trend of pore evolution to the annealing temperatures. A very low porosity of 0.5% with 14nm APD is calculated from the NSO sample annealed at 800 ℃. As the annealing temperature increase, more open pores are formed in the silicon film and both the porosity and pore size increase rapidly. The porosity increases to 14% and the APD goes up to 24.7nm when the annealing temperature goes up to 1100 ℃. The pore distribution plot in figure 4-4 (c) shows that pores in the NSO system shifts to large size with higher density and the size distribution becomes boarder as the annealing temperature increases.

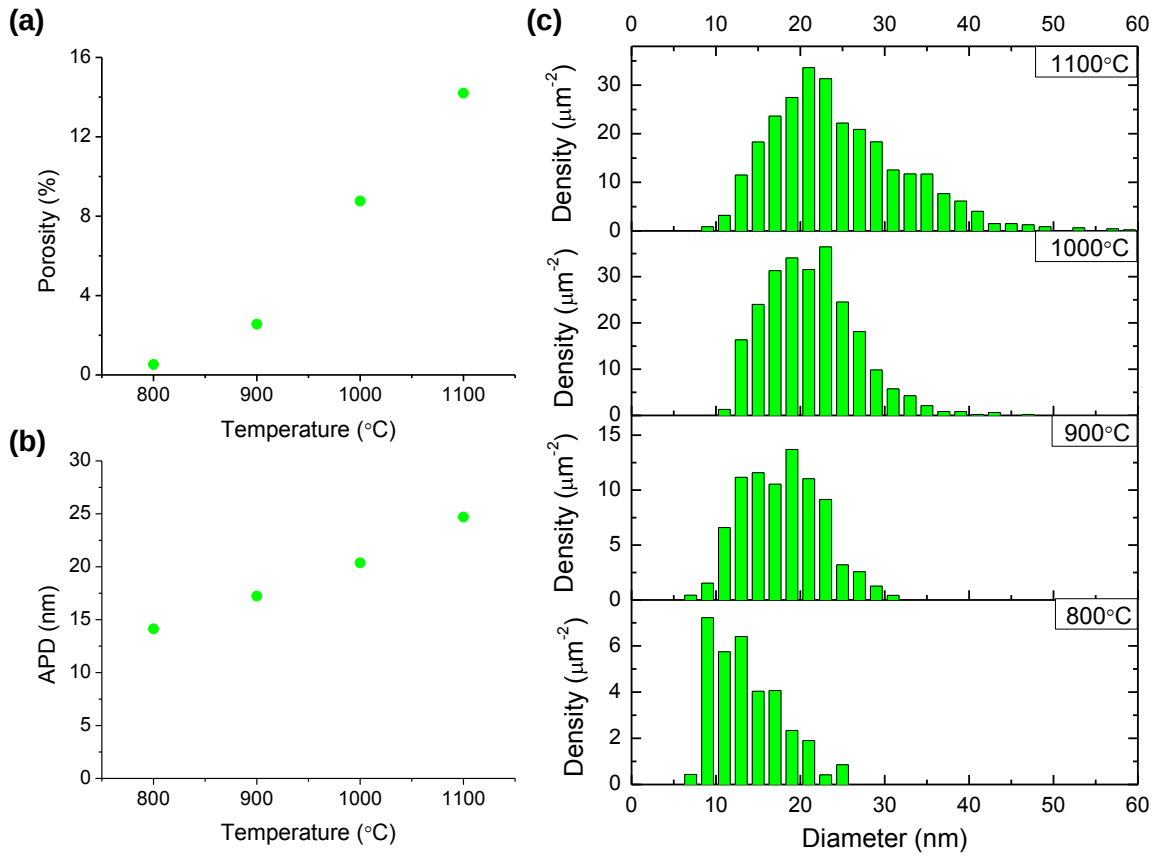


Figure 4-4 Pore characteristic plots of the NSO system after RTP annealing, a) porosity, b) APD and c) pore size distribution.

4.2.3 Pore Formation in the OSN Stack

The only difference between the OSN and NSO systems is the deposition order. Their deposition orders are opposite with each other. Figure 4-5 shows TEM images of the OSN system with nanopore formation after the rapid thermal annealing. Apparently pores are formed in both systems, however, the pore characteristics are not exactly same in these two systems.

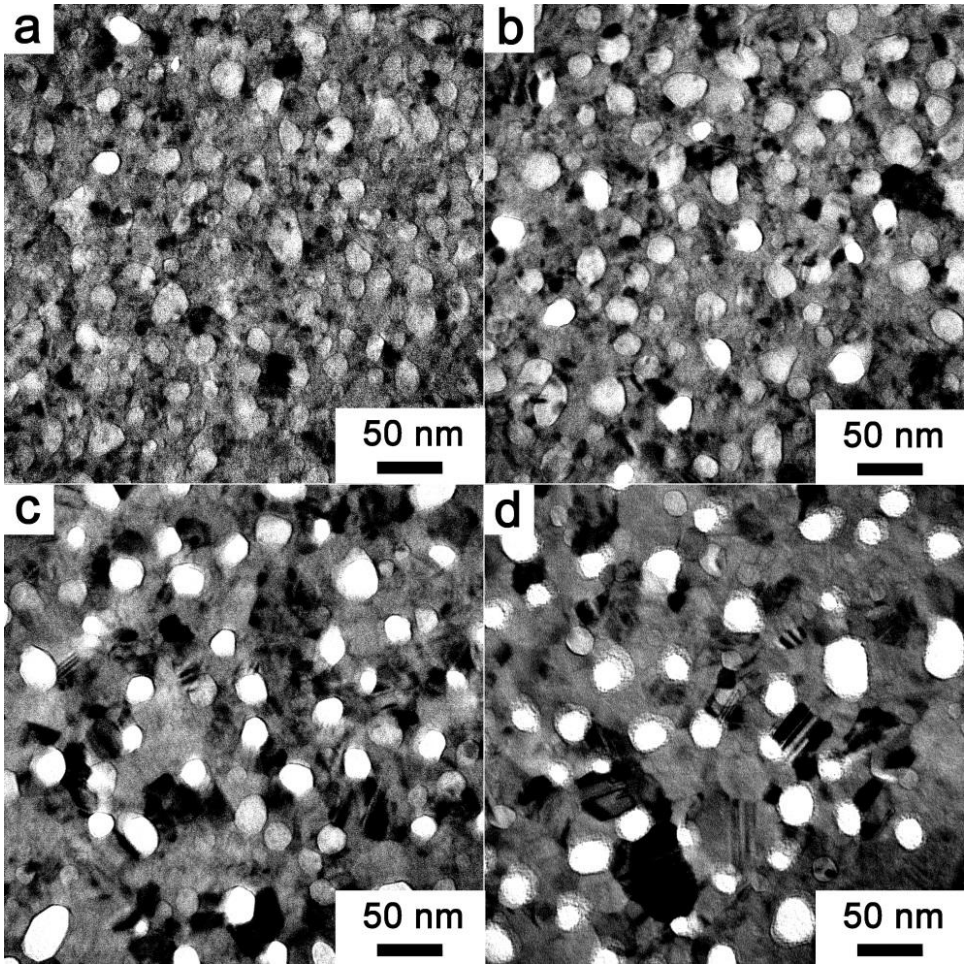


Figure 4-5 TEM images of the OSN system after RTP annealing at a) 800 ℃, b) 900 ℃, c) 1000 ℃ and d) 1100 ℃.

Figure 4-6 shows the pore characteristics of the OSN systems including porosity, APD and the pore size distribution. In the porosity plot, the OSN system also begins with a low porosity of 0.2% with 11nm APD when annealed at 800 ℃. The porosity jumps from 2% to 9% as the annealing temperature increases from 900 ℃ to 1000 ℃ and reaches to 12% at 1100 ℃. The APD increases steady with the temperature and reaches to 21.4nm at

1100 ℃. The pore distribution plot confirms this steady increase of pore size and pore density with the annealing temperatures.

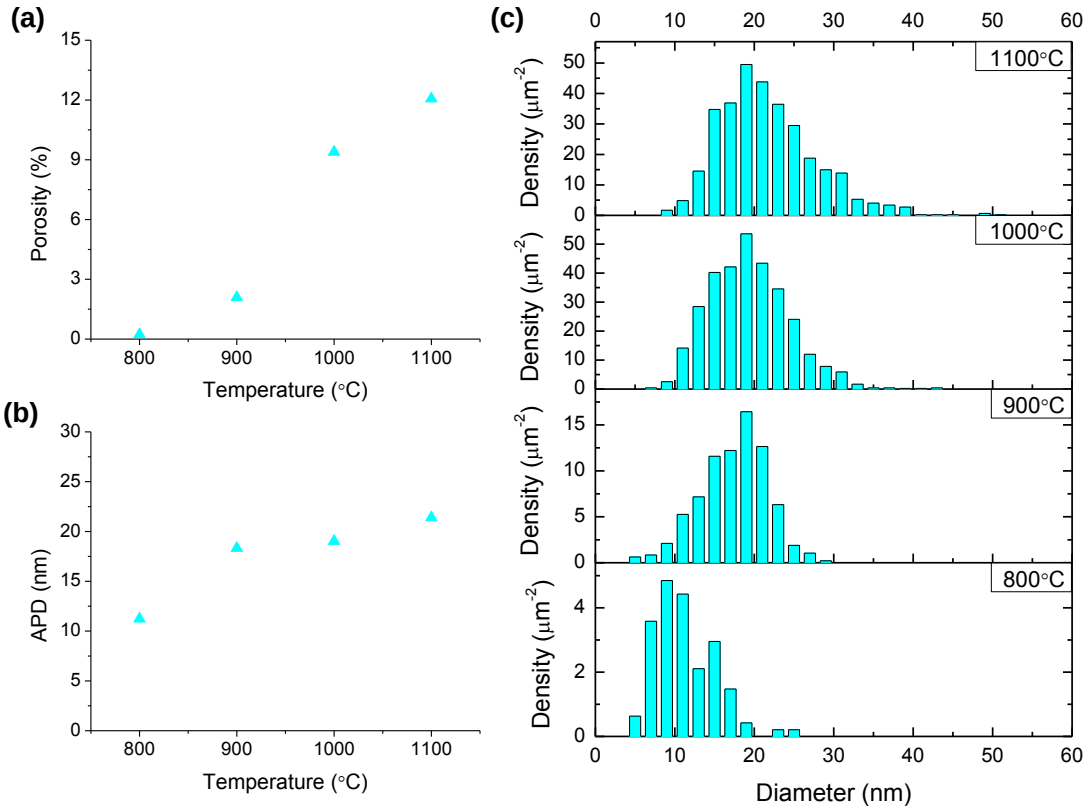


Figure 4-6 Pore characteristic plots of the OSN system after RTP annealing, a) porosity, b) APD and c) pore size distribution.

4.2.4 Pore Formation in the OSO Stack

OSO stack, as the control sample, shows different pore morphologies after the rapid thermal annealing. Figure 4-7 shows TEM images of annealed OSO stacks at different temperatures. Very limited through pores are observed in OSO samples when the annealing

temperature is below 1000 ℃. The porosity plot from figure 4-8 confirms that the porosity is below 0.5% at these two annealing temperatures. Open pores with large size are observed in OSO samples when the annealing temperature increases to 1000 ℃ and above. The porosity goes from 1% to almost 4% as the annealing temperature increases from 1000 ℃ to 1100 ℃. Correspondingly, the APD increases from 24.2nm to 30.7nm. The pore size distribution plot clearly shows this rapid increase of pore size with the annealing temperature in the OSO system.

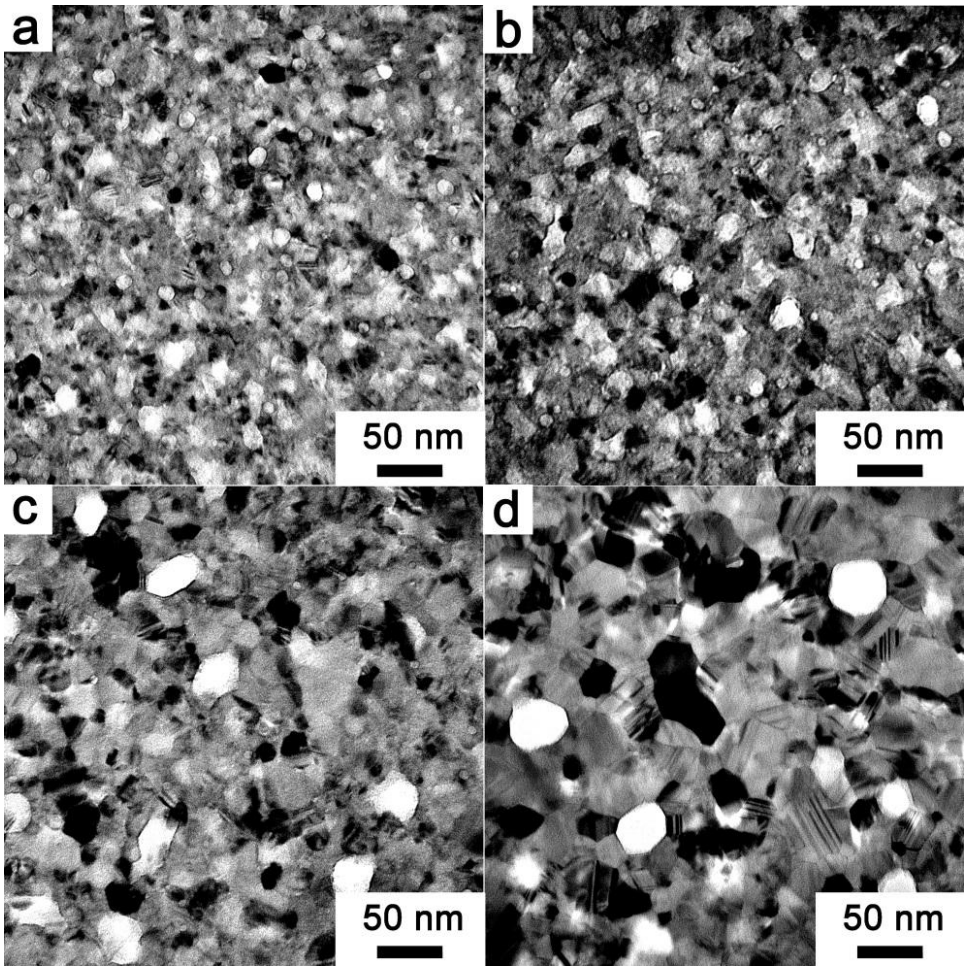


Figure 4-7 TEM images of the OSO system after RTP annealing at a) 800 ℃, b) 900 ℃, c) 1000 ℃ and d) 1100 ℃.

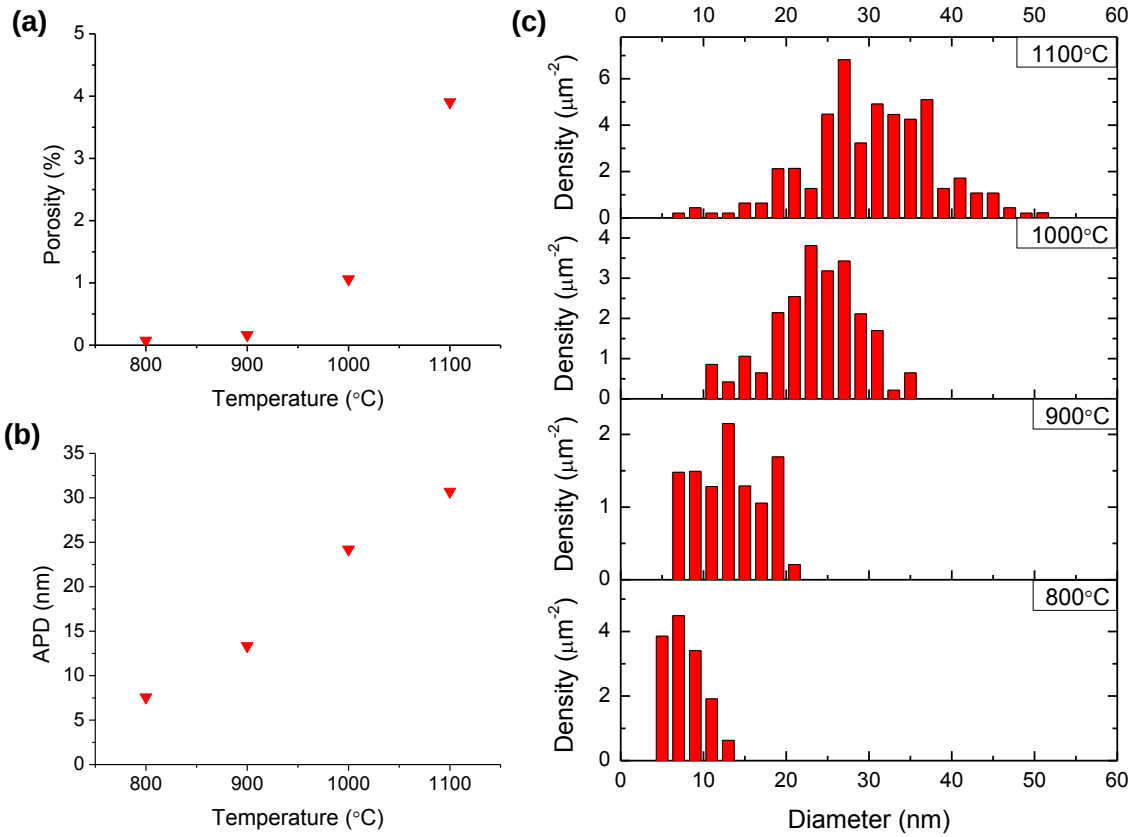


Figure 4-8 Pore characteristic plots of the OSO system after RTP annealing, a) porosity, b) APD and c) pore size distribution.

4.2.5 Pore Characteristics Comparison in Four Stacks

Pores are able to form in silicon films even though the capping layer switches from silicon dioxide films to silicon nitride. However, the capping layer materials greatly affect

the pore formation process and the resultant pore characteristics. To further study this effect, pore characteristics from these four systems are compared in details.

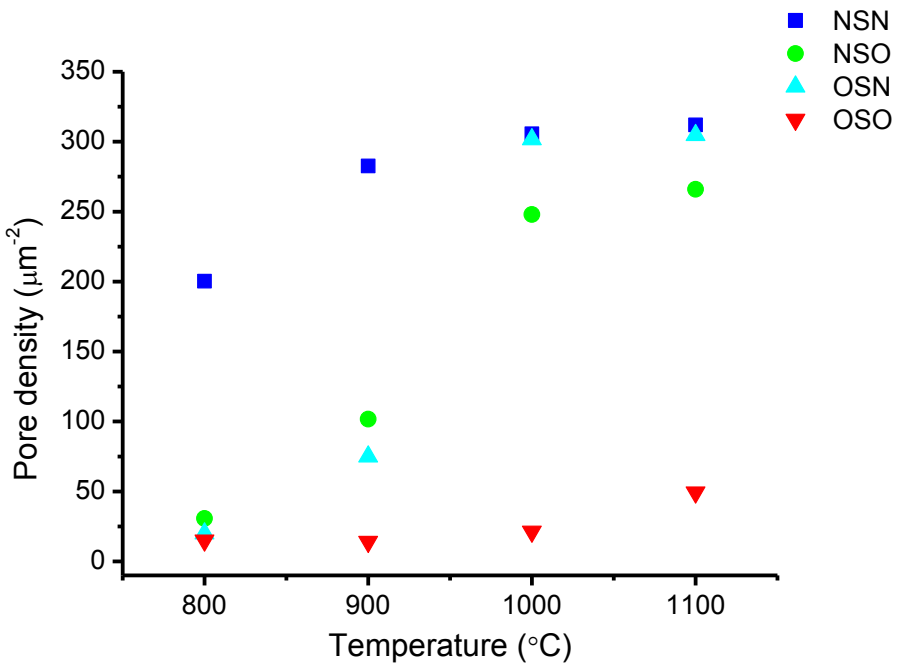


Figure 4-9 Pore density for the four systems as a function of the annealing temperature.

Figure 4-9 compares the pore density of four systems as to the annealing temperature. The pore density in the NSN system, which stays the highest among the four systems for all annealing temperatures, is already high at 800 ℃, increases gradually with temperature and appears to saturate at 1000 ℃. The pore density in the OSO system, which remains the lowest among the four systems for all annealing temperatures, is very low at 800 ℃, changes little until the annealing temperature reaches 1000 ℃ and increases slightly at 1100 ℃. Even at 1100 ℃ the pore density of the OSO system is 5 to 6 times lower than for the other three systems. The OSN and NSO systems also start with very few pores at 800 ℃,

however, the pore density increases rapidly as the annealing temperature increases. The pore density of the OSN system exceeds that of the NSO system at 1000 ℃ and reaches that of the NSN system at 1100 ℃. This comparison shows that high density pores can be formed in Si films in the OSN, NSO and NSN systems at high annealing temperature. The pore formation in the Si film is greatly enhanced by the existence of even a single silicon nitride capping layer.

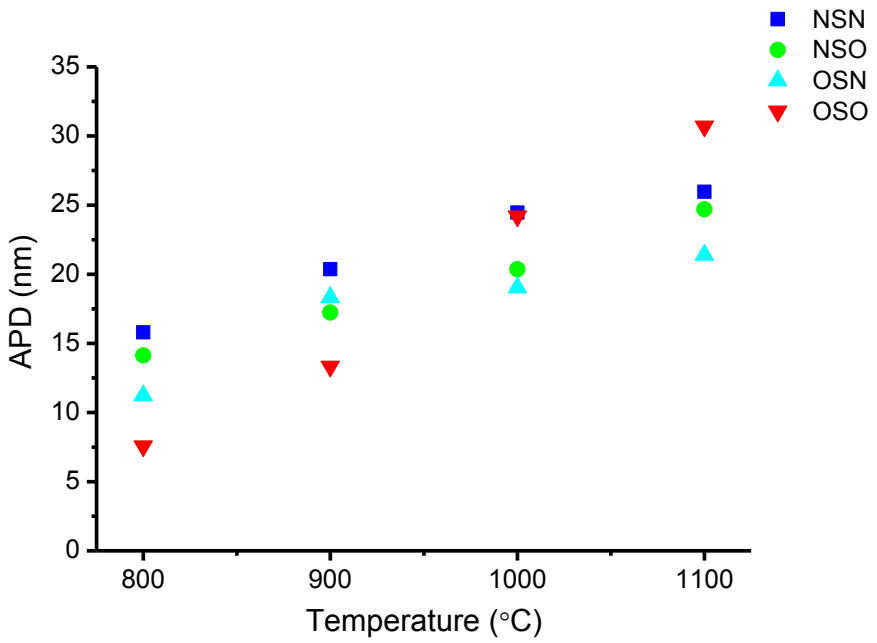


Figure 4-10 APD comparison for the four systems as a function of the annealing temperature.

Figure 4-10 compares the average pore diameter (APD) of the four systems. The differences in the APD among these four system are not large as for the pore density. The NSN system yields slightly larger APD among four systems when the annealing temperature is below 1000 ℃. The APDs in the OSN and NSO systems are smaller than in

the NSN system for all temperatures. The APD for the OSO system is the smallest at 800 ℃ but it increases rapidly, becoming the largest at 1100 ℃. This can be understood by plotting the pore distribution. Figure 4-11 shows the pore distributions of the four systems at 1100 ℃. In the OSO system, the pore density is not high but the majority of the pores are from 24nm to 38nm in diameter. In the NSN system, the pore density is much higher than that of the OSO system but the majority of the pores are from 20nm to 30nm in diameter. The pore distributions of the OSN and NSO systems yield slightly smaller pores compared to the NSN system.

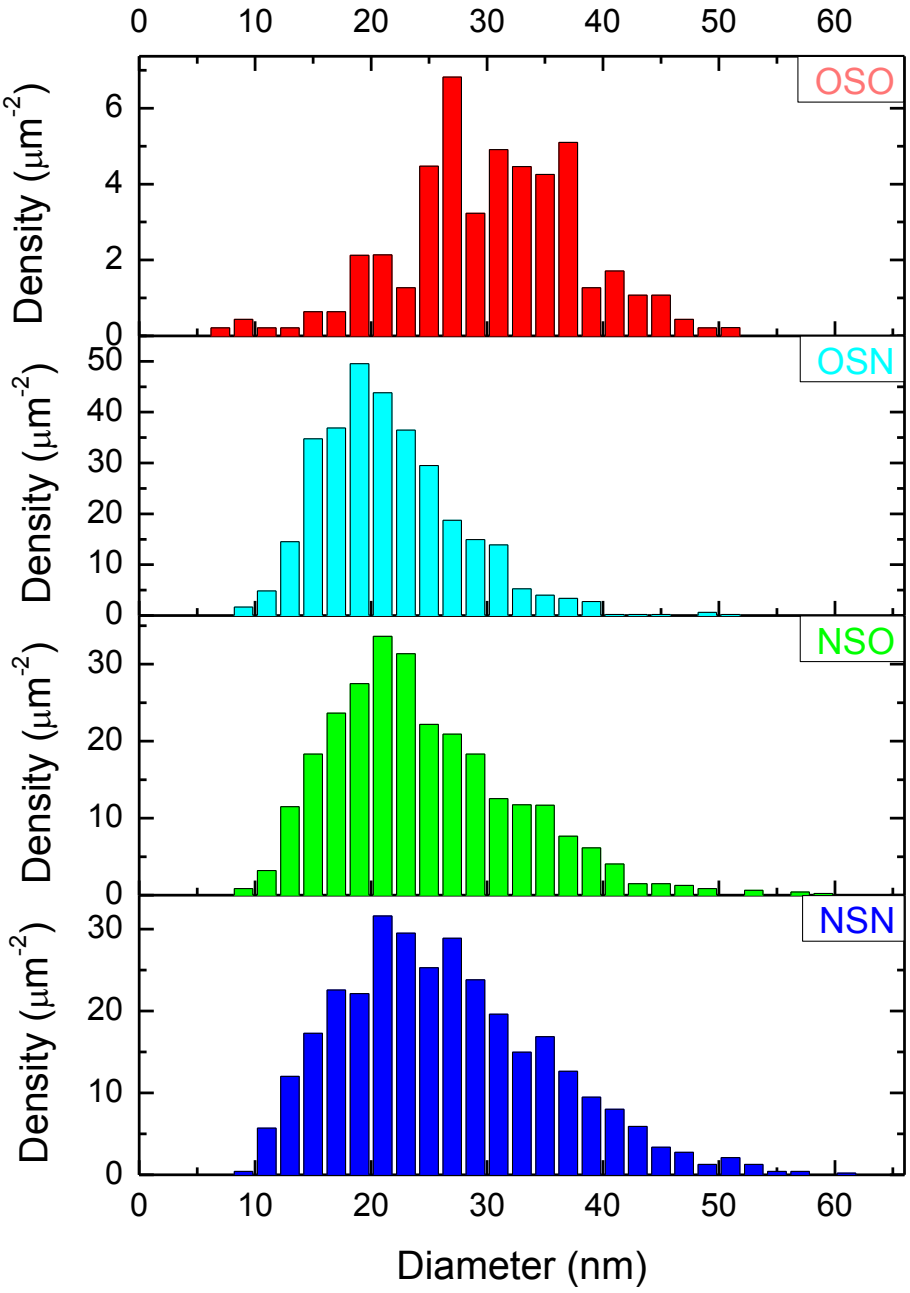


Figure 4-11 Pore distribution comparison of the NSN, NSO, OSN and OSO systems after annealing at 1100 ℃. Note that the vertical scales on the four panels are different.

Figure 4-12 compares the pore distribution of the OSO and NSN systems at four different annealing temperatures. In the OSO system, as the annealing temperature increases, the pore size distribution quickly shifts to larger diameters without significantly increasing the total pore density. This indicates that pore growth rather than new pore formation donimates the pore evolution process in the OSO system. The NSN system, however, shows a different pore evolution. With increasing annealing tempreature, the pore distribution slowly shifts to the large pores. At the same time, the density of relatively small pores (<20nm) remains high. This indicates that new pore formation plays a big role in the pore evolution of the NSN system at higher annealing temperatures.

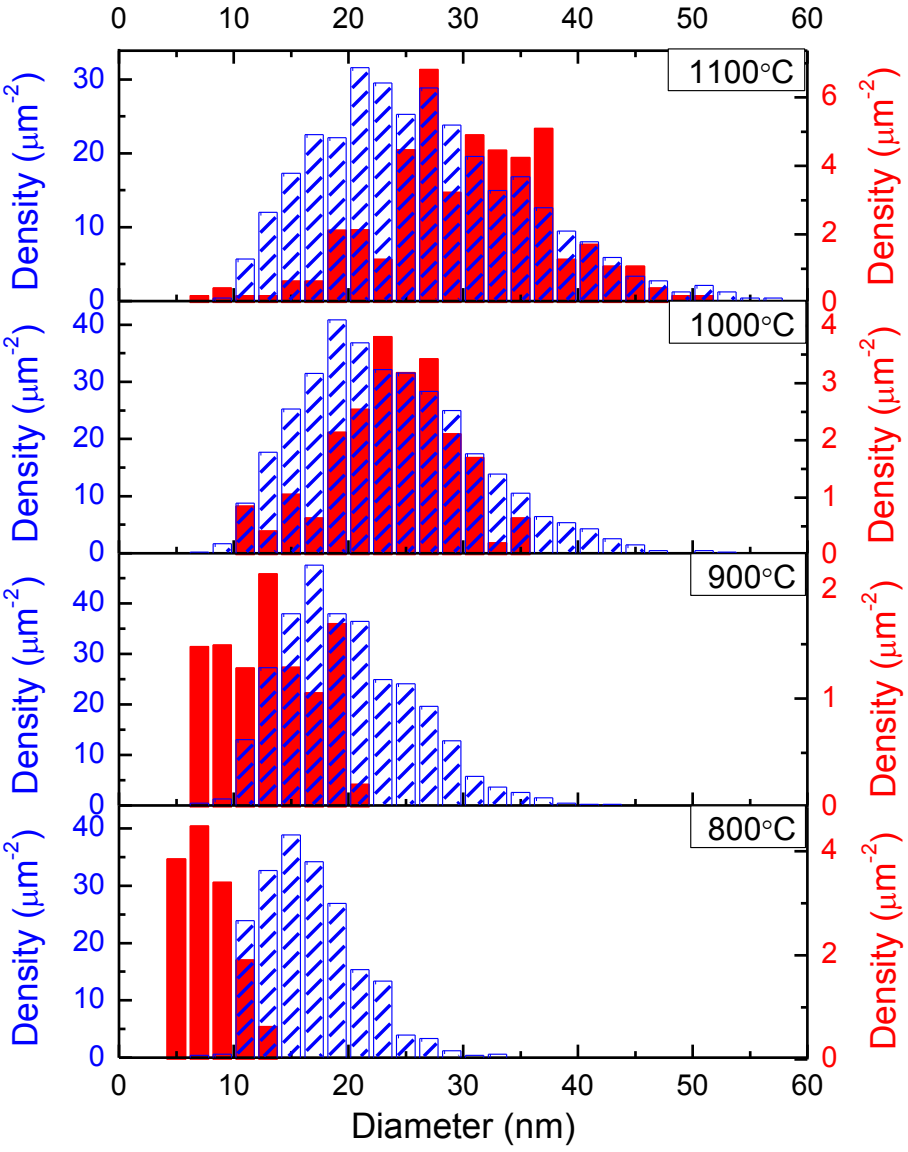


Figure 4-12 Pore distribution comparison for the OSO and NSN system at four different annealing temperatures; the blue color represents the NSN system and the red color represents the OSO system. Note that the left and right vertical scales on the four panels are different.

Figure 4-13 compares the porosity among the four systems. The NSN system yields the highest porosities at all temperatures. The porosity increases rapidly with the annealing temperature and reaches 20% when the NSN system is annealed at 1100℃. In contrast, the porosity in the OSO system stays the lowest among the four systems at all annealing temperatures. It increases very slowly when the annealing temperature is below 1000℃. Even at 1100℃, the porosity is only 3.8%. The porosities in the OSN and NSO systems start low at 800℃ and increase quickly with annealing temperature. They stay between those of the NSN and OSO systems at all annealing temperatures. Consistent with our previous observation, the large difference in porosity between the NSN and OSO systems is due to the pore density. At higher annealing temperatures, the NSN system produces not only larger but denser pores while only a limited number of larger pores are formed in the OSO system. In other words, pore formation is enhanced in silicon films when sandwiched by silicon nitride layers compared to silicon dioxide layers, yielding the highest pore density and porosity. This highly porous Si membrane from the NSN stack is very promising for filtration applications since a large number of relatively big pores would enhance the fluid flow through the membrane.

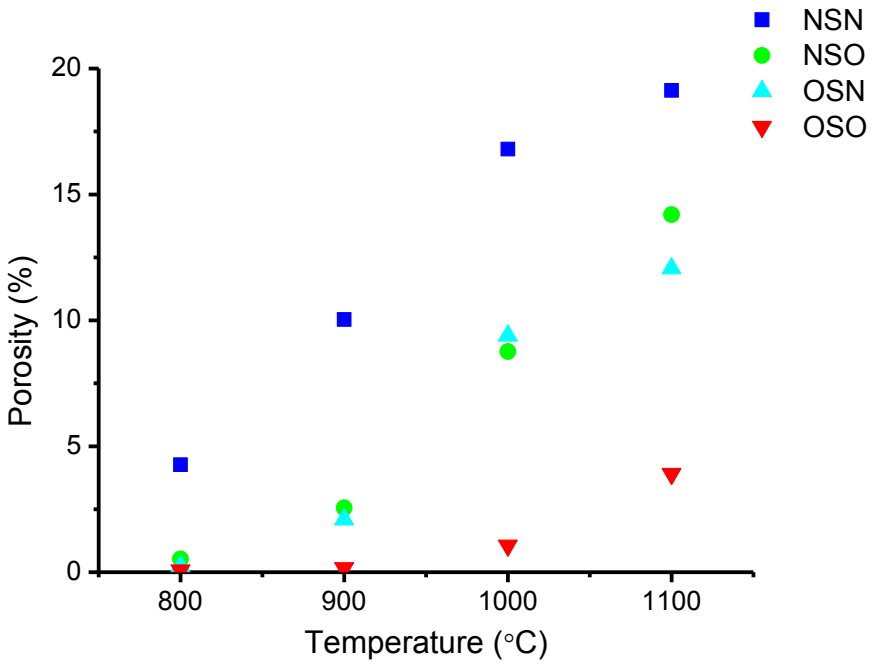


Figure 4-13 Porosity comparison for the four systems as a function of the annealing temperature.

4.3 NSN Stacks with Different Thick Si Films

It has been shown that pore formation in the NSN stack is greatly enhanced compared to the OSO stack. To further explore pnc-Si membranes with higher porosity and bigger pores for a broad range of separation applications, NSN stacks with different thick silicon films have been tested. Silicon films with different thicknesses ranging from 7nm to 10nm, 15nm, 25nm, 50nm and 100nm are sandwiched by two 30nm thick silicon nitride layers. All samples are annealed at 1000 ℃ with a ramp rate of 50 ℃/s inside the RTP. The soaking time is 1 minute at 1000 ℃. Figure 4-14 shows TEM images of annealed samples.

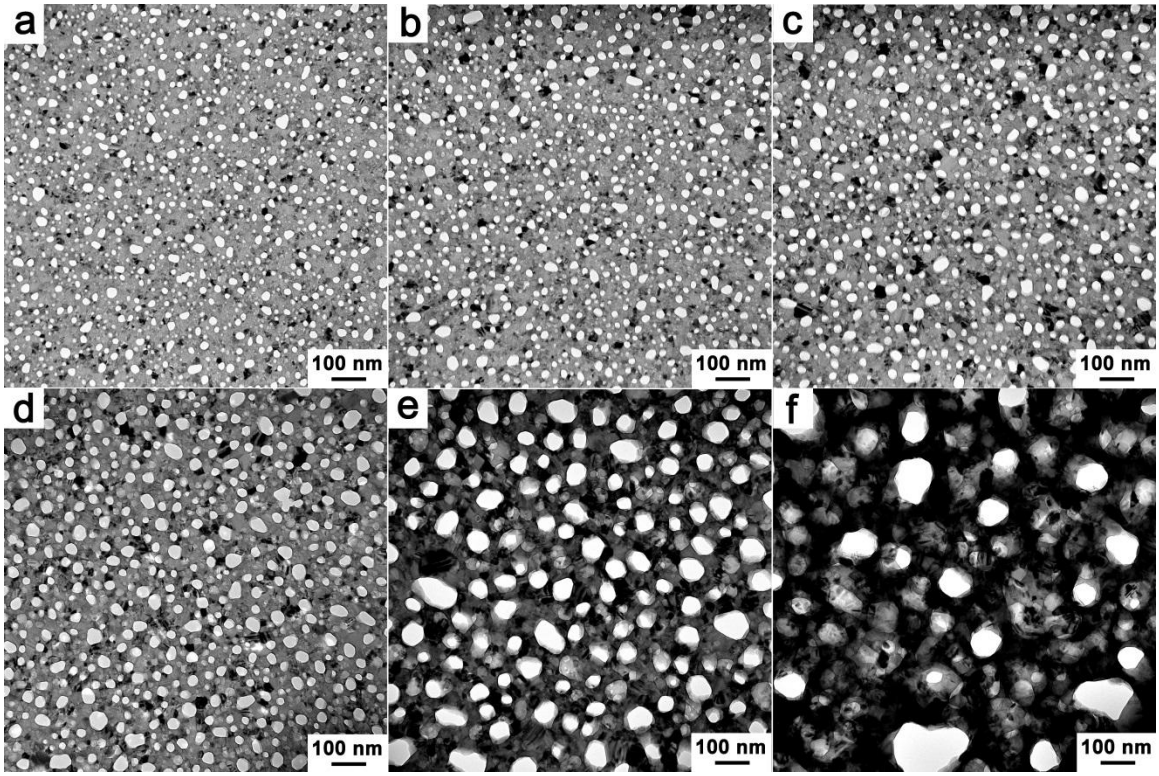


Figure 4-14 TEM images of annealed NSN samples with different thick silicon film, (a) 7nm, (b) 10nm, (c) 15nm (d) 25nm, (e) 50nm and (f) 100nm.

Pores are formed in all silicon films after the rapid thermal annealing. This is the first time that pore formation is observed in a 7nm thick silicon film from the NSN stack since previous experiment showed no through pores are identifiable in a 9nm thick silicon film from the OSO stack after annealing.[58] Pores become bigger as the silicon film goes thicker, which is in consistent with our previous result.[53]

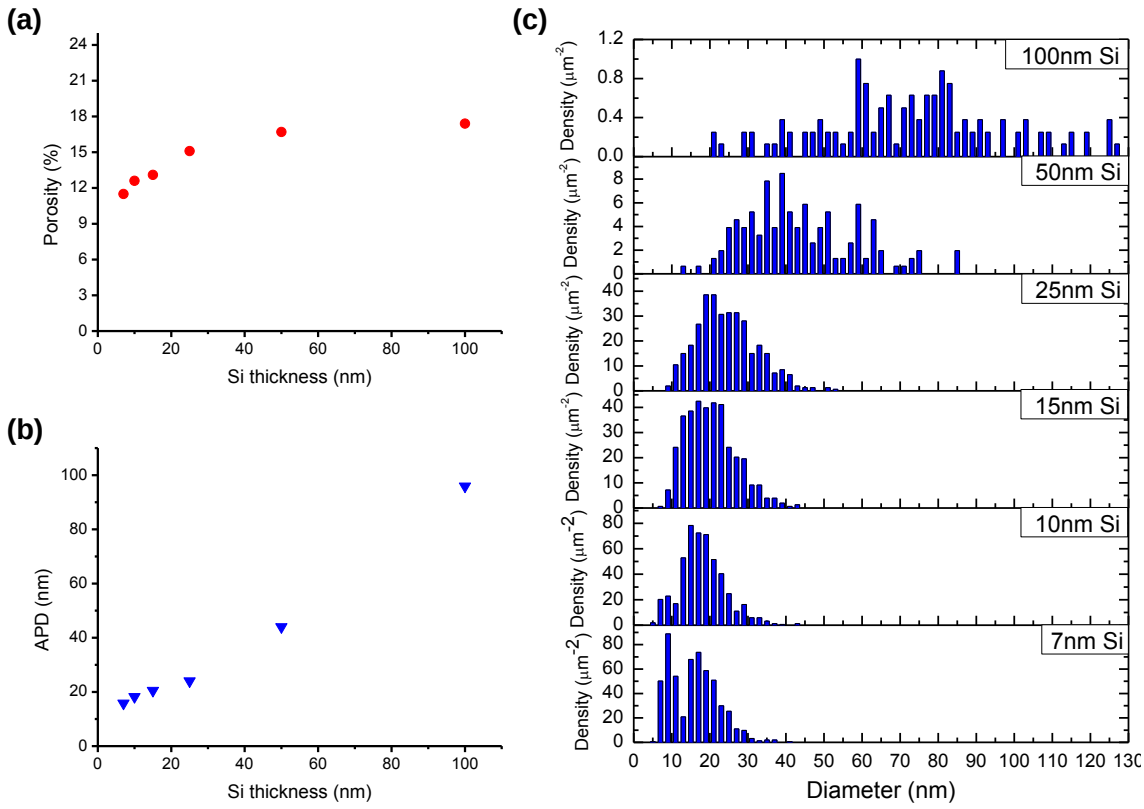


Figure 4-15 Pore characteristics of the annealed NSN stacks with different thick silicon films, (a) pore density, (b) APD, and (c) pore distribution.

Figure 4-15 compares the pore characteristics from the annealed NSN stacks with different thick silicon films. The porosity increases with the silicon thickness gradually and starts reaching saturated around 17% as the silicon film increases to 50nm. The APD gradually increases with the silicon thickness at beginning and then rapidly when the silicon film passes 50nm thick. The pore distributions from thin silicon samples (<25nm) are very different from those of thick silicon samples (≥50nm). Especially the pore distribution of 100nm silicon sample shows a very broad size distribution from about 20nm to 120nm in diameter.

Another interesting morphology is that pits feature start to show up in the silicon film as it becomes thicker. This makes sense because silicon nanocrystals are restricted to a single layer when the silicon film is very thin and it is relatively easy for voids to span the entire thickness of the film leading to a through pore. As the silicon film becomes bigger, silicon nanocrystals are no longer confines in the thickness direction and can be grown to multilayers. It would result lots of voids or pits feature rather than through pores. The SEM image of 100nm thick silicon sample from the NSN stack in figure 4-16 confirms the voids and pits morphology. The top-down view clears shows that lots of pits and some pores are formed in silicon film after annealing. The cross-sectional view confirms that these pits are not spanning through this thick silicon film. Those that stay inside the silicon film are voids and those that stay in surface are pits. When they meet and go through the silicon film, they become pores. It also shows that the thickness of the silicon film expands as it becomes porous which is in consistent with mass conservation.

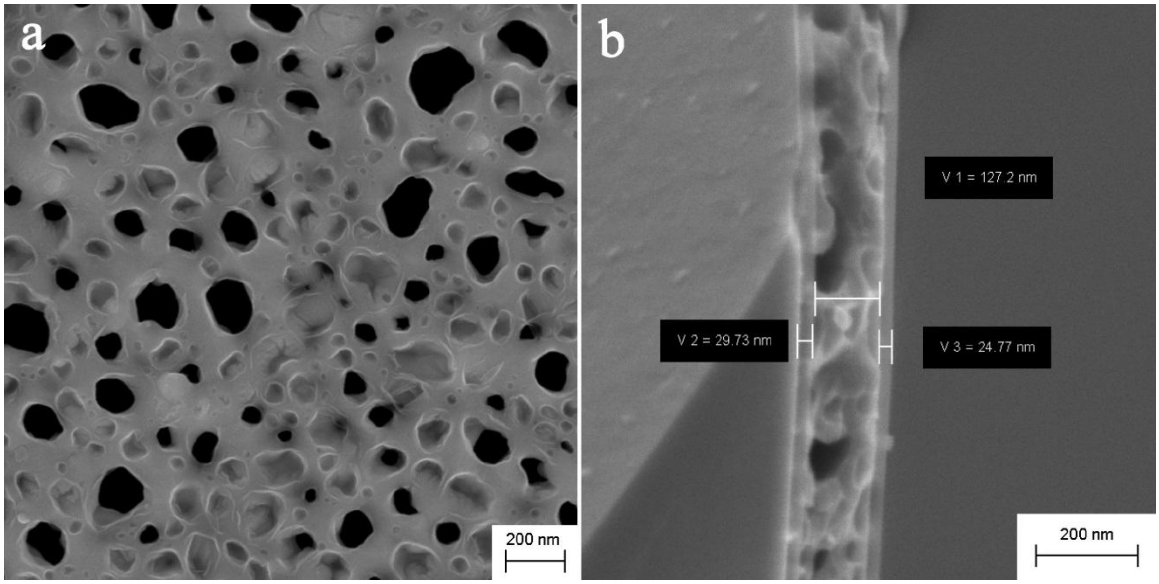


Figure 4-16 SEM images of 100nm pnc-Si membrane from the NSN stack, (a) top-down view and (b) cross-sectional view.

Since pits become dominant morphology in thicker silicon film in the NSN stack, it is possible that the actual porosity maybe lower compared to the result from the image processing with Matlab script. This is because the image processing relies on the image contrast of pores with non-porous area. However when the silicon film goes thicker, the non-porous area becomes darker, which increases the contrast of non-porous areas with pores. This also increases the contrast between non-porous areas with pits area, which may result over large porosity. So we use permeance measurement to verify the porosity for thicker (≥50nm) pnc-Si membranes as our previous permance results [84] showed a very good consistency with the image processing result for porosity when the silicon film is below 30nm. The permeance result shows that the actual porosities for 50nm and 100nm pnc-Si membranes from the NSN stacks are 9.1% and 7.2%, which indeed supports that the actual porosity is over quantified due to the surface pits.

Though the actual porosity from permeance measurement is lower than that from the image processing, through pores are still able to form in 100nm thick silicon film from the NSN stack. However, pits, instead of through pores, dominate the morphology in 100nm thick silicon film from the OSO stack.

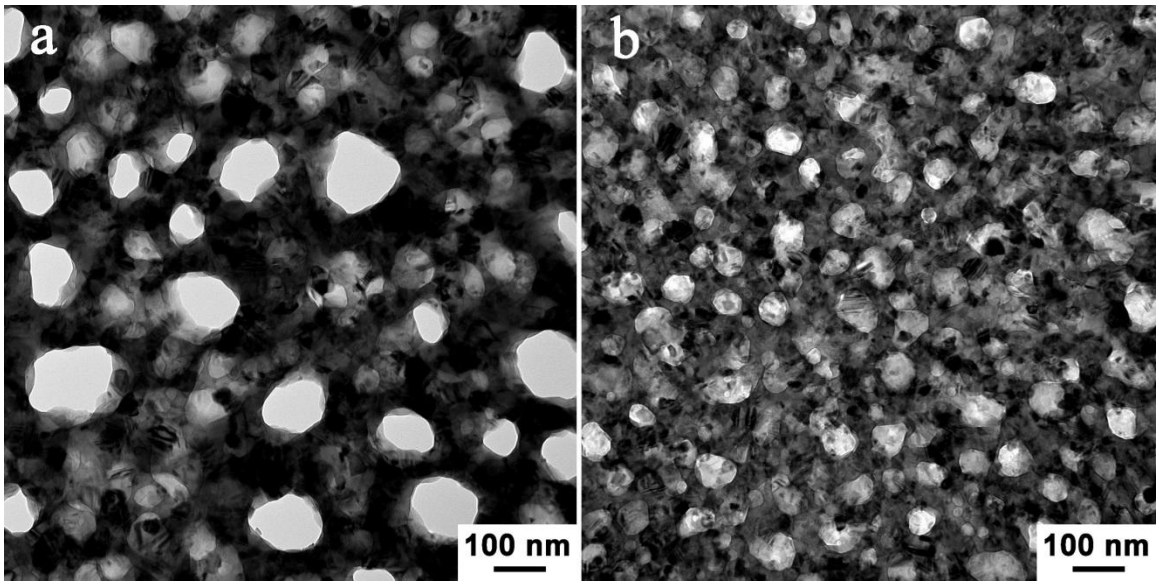


Figure 4-17 TEM images of annealed 100nm Si film from (a) the NSN stack, and (b) the OSO stack

Figure 4-17 compares the TEM images of annealed 100nm Si films from the NSN and OSO stacks. Voids and pits are dominant features in the silicon film from the OSO stack. Few open pores can be observed from the TEM image in the OSO sample where they are quite obvious in the NSN sample. This result also supports that pore formation is enhanced in the NSN stack.

It has been reported that the type of interface would influence the crystallization behavior of amorphous silicon.[85, 86] As the NSN and OSO systems have different interfaces, it is likely that the crystallization of our amorphous silicon films would be affected by different interfaces in these two systems. A possible explanation for the pore formation enhancement in the NSN system might be found in the interface energy difference between silicon/silicon nitride and silicon/silicon dioxide [86-89].

4.4 Conclusion

In this chapter, for the first time it is found that nanopores can be formed in an amorphous silicon film sandwiched by two silicon nitride films during a rapid thermal annealing. This discovery introduces a new control variable for pnc-Si membrane fabrication, demonstrating new properties in the expanded NSN materials system. Four different systems including NSN, NSO, OSN and OSO have been tested. It is found that the NSN system produces the highest porosity and pore density after annealing, while the OSO system produces the lowest. The porosity and pore density of the mixed OSN and NSO systems fall between those with matched barrier layers. NSN stacks with different thick silicon films have also been tested. Pore size and porosity increase with the silicon film thickness. Pits start to show up in silicon film when it passes 50nm. Through pore are observed in 100nm silicon film from the NSN stack where pits are dominant features in 100nm silicon film from the OSO stack. This indicates that pore formation is enhanced in the NSN stack and the enchancement may be due to the difference in interfacial energy between silicon/silicon dioxide and silicon/silicon nitride.

Chapter 5 Ex-situ and In-situ Annealing Study of Pore Formation

5.1 Overview

In this chapter, silicon crystallization and pore formation is studied by TEM using ex-situ and in-situ annealing techniques. Both the OSO and NSN stacks are ex-situ and in-situ annealed to introduce pore formation in silicon films. Silicon crystallization and associated pore formation process are directly observed with in-situ heating in a TEM chamber. Detailed pore formation process and related discussions are presented.

5.2 Pore Formation Temperature

Achieving a basic understanding of the pore formation in pnc-Si membranes is extremely important to control the pore characteristic for different membrane applications. It has been found that pore formation is always associated with crystallization of the silicon film. This indicates that pore formation is directly driven by thermal energy, or the annealing temperature. A series of annealing experiments on the OSO stack have been conducted with different annealing temperatures to investigate the pore formation initiation temperature. The ramp rate (50 ℃/s) and the soaking time (1 minute) are the same for all samples. In this OSO stack, the silicon film is 15nm and the capping oxide layers are both 20nm. Figure 5-1 shows TEM images of the OSO stack pre and post annealing at 600 ℃.

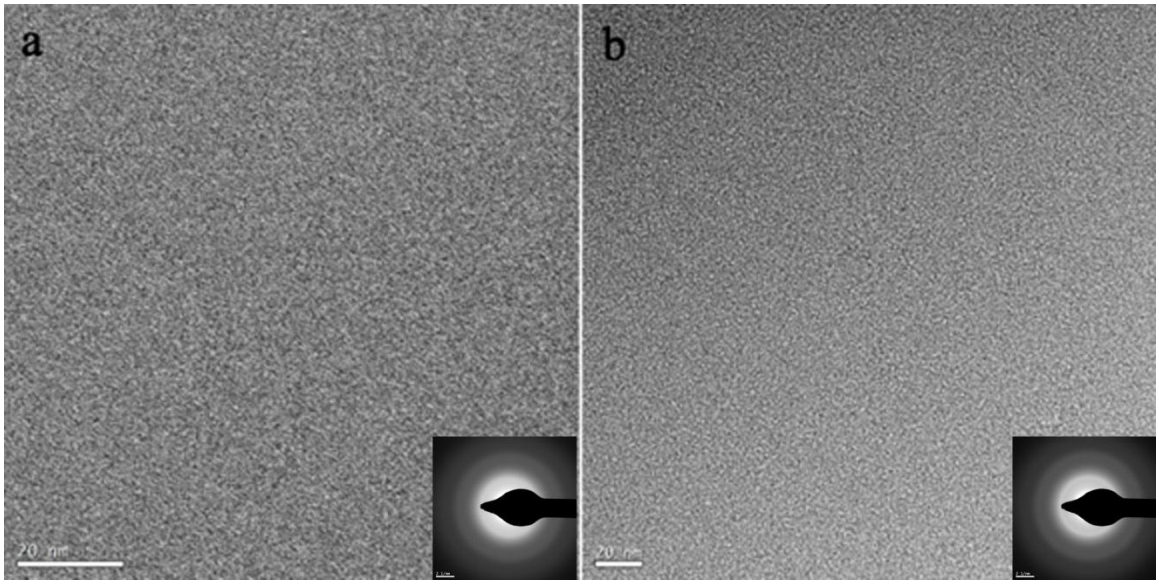


Figure 5-1 TEM images of the OSO stack pre (a) and post (b) annealing at 600 ℃.

. No silicon crystals or pores are observed in the silicon film after annealing at 600 ℃. The silicon film appears featureless consistent with their amorphous nature and electron diffraction image confirms that annealing at 600 ℃ for 1 minute is not enough to introduce solid phase crystallization of the silicon film. It also confirms that pores are not be formed in the silicon film if crystallization does not take place.

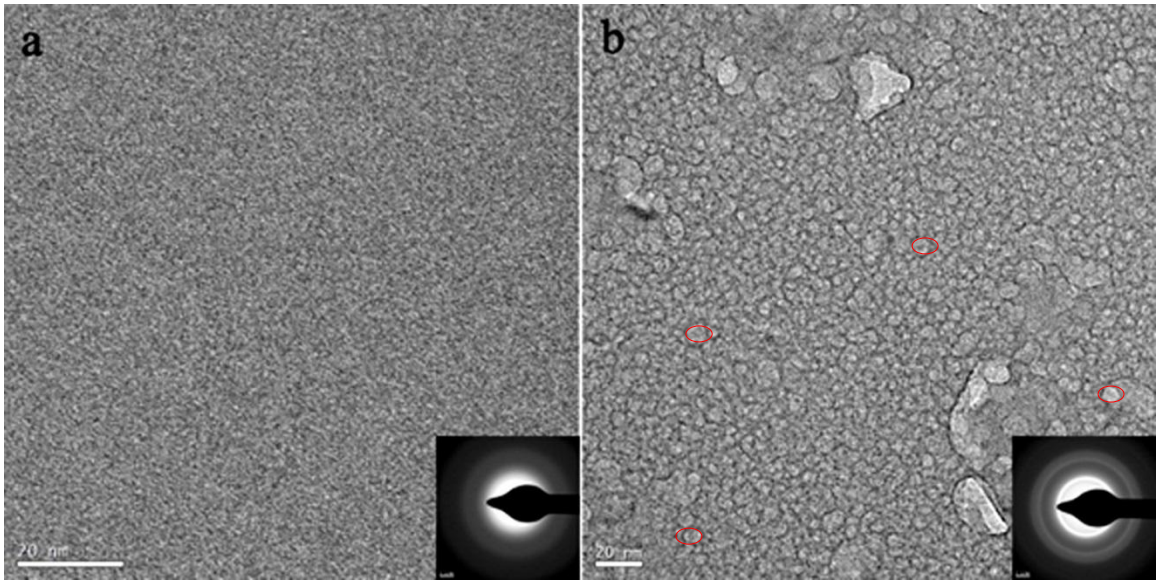


Figure 5-2 TEM images of the OSO stack pre (a) and post (b) annealing at 680 ℃.

Figure 5-2 shows the TEM images of the OSO stack pre and post annealing at 680 ℃. A few pores and silicon nanocrystals are observed in the silicon film after annealing. New features reminiscent of a "honeycomb" (with red circles) can be seen in the silicon film even through it is still amorphous. We believe that this feature may represent nano-pits or nano-voids structure in the silicon film. Very dim polycrystalline rings can be seen from the electron diffraction image, which also confirms that the majority of the silicon film is still amorphous. This indicates that a very partially crystallized silicon film with a few pores is achieved at this temperature.

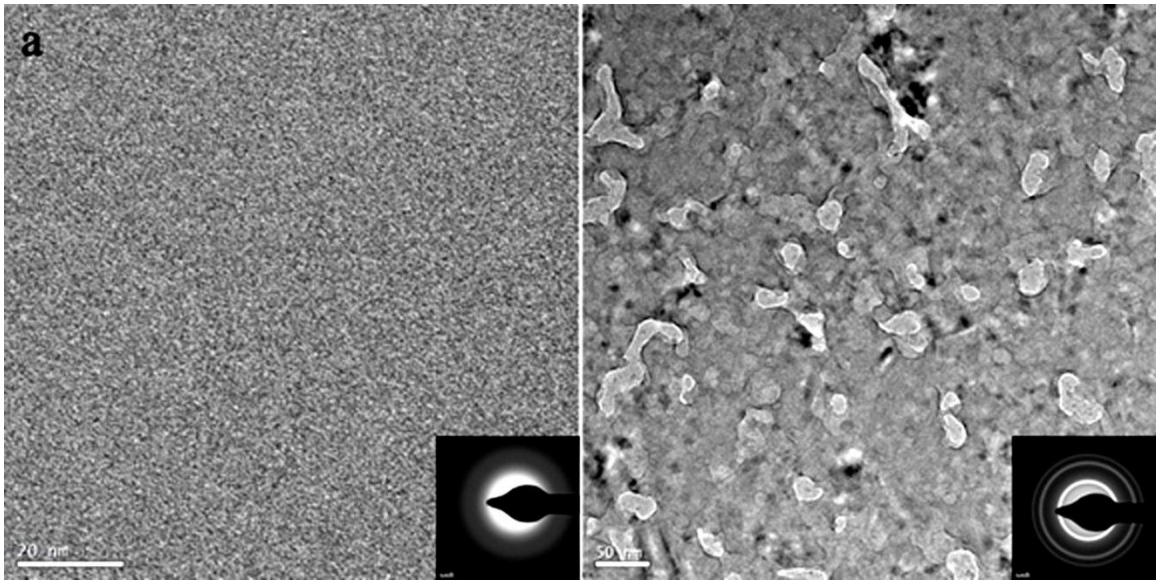


Figure 5-3 TEM images of the OSO stack pre (a) and post (b) annealing at 700 ℃.

Full crystallization of the silicon film is observed after annealing at 700 ℃. Figure 5-3 shows a TEM image of a crystallized silicon film with pores after annealing at 700 ℃. The diffraction image clearly shows polycrystalline ring features. However, the shape of the pores is very irregular. Some of these irregular pores resemble elongated rods and others have very irregular shapes. The pore shapes suggest that they may result from the coalescence of pores that are adjacent to each other. This pore formation temperature experiment suggests that annealing temperatures from 680 ℃ to 700 ℃ would be a good starting point for detailed ex-situ and in-situ annealing studies.

5.3 Ex-situ Heating Study of Pore Formation

Since pore formation is always associated with the crystallization of the silicon film, it is necessary to study the crystallization process of the silicon film to understand pore

formation. The ex-situ heating experiment is designed to investigate silicon crystallization process. The previous experiments have shown that silicon crystallization and pore formation take place at around 700 ℃ during rapid thermal annealing. So we choose this temperature for ex-situ heating experiments in both the OSO and NSN stacks. The silicon film thickness in these two stacks is kept at 25nm and the capping layers (nitride and oxide) at 30nm. Samples are heated to 700 ℃ with a 50 ℃/s ramp rate and then stay at 700 ℃ for different time durations (1s, 5s, 10s, 30s and 60s).

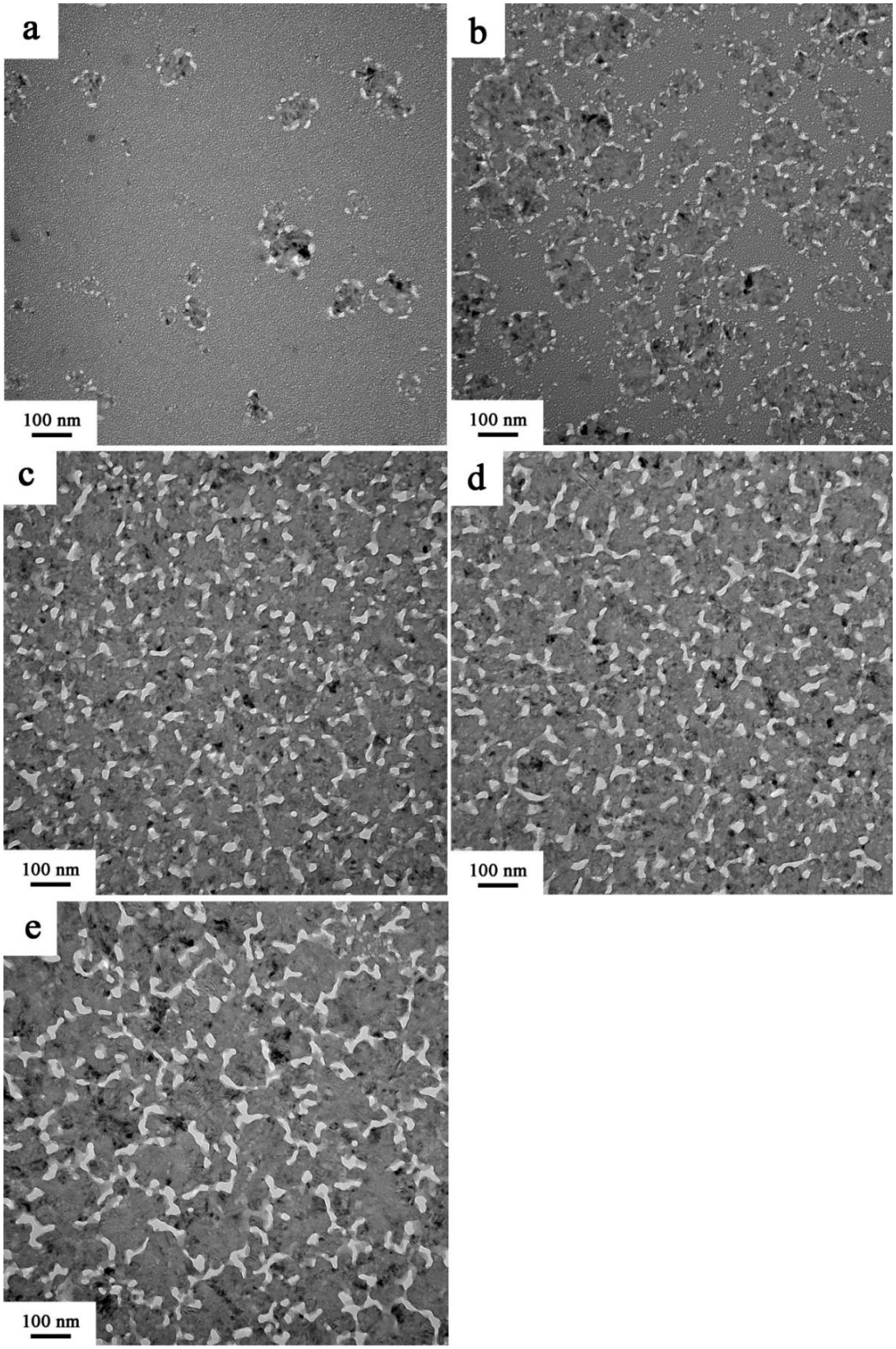

a
100 nm
b
100 nm
c
100 nm
d
100 nm
e
100 nm

Figure 5-4 TEM images of the NSN stacks annealed at 700 ℃ for (a) 1s, (b) 5s, (c) 10s, (d) 30s and (e) 60s.

Figure 5-4 shows the ex-situ heating result of the NSN stacks at 700 ℃ for different time durations. The TEM images clearly capture the onset of pore formation in the NSN stacks. After 1s annealing at 700 ℃, we observe a few silicon nanocrystals all surrounded by pores. The pores are arranged among the silicon nanocrystals in a 'pearl necklace pattern', and they barely touch each other. At this stage, the majority of the silicon film is still amorphous. Incubation and nucleation dominate the crystallization process of the silicon film. When the annealing time increases to 5 seconds, 'pearl necklaces' around silicon nanocrystals are formed in most of the silicon film. Some pearl necklaces merge with adjacent ones to form bigger pearl necklaces. The density of both the silicon nanocrystals and pores increases significantly as the annealing time increases from 1s to 5s. It indicates that the silicon nucleation and pore formation rates are very fast since the difference between the figure 5-4a and 5-4b is only 4 seconds between these two intervals.

After annealing at 700 ℃ for 10s, silicon nanocrystals and the nanopores are all over the silicon film. 'Pearl necklace' features are no longer apparent, which is probably due to completion of the silicon crystallization and coalescence of nanopores. The coalescence of nanopores is quite obvious in figure 5-4c, which could be the reason for the irregular shapes of nanopores. In addition to irregular pores, we also observe a lot of small isolated round pores. The average size of the irregular pores is bigger than in the previous two pictures. The majority of the silicon film is in nanocrystalline phase. This means that the nanocrystal

nucleation stage is already complete after 10s. Nanopores coalesce with adjacent ones during this period. When the annealing time is even longer, for example, 30 seconds or 60 seconds, the morphology of the films change relatively little. However, it seems that the small round pores gradually disappear with longer annealing time. As a result, the size of the irregular pores, which are believed to represent the final shape of coalesced pores, become bigger with annealing time. The size of silicon nanocrystals also increases with the annealing time.

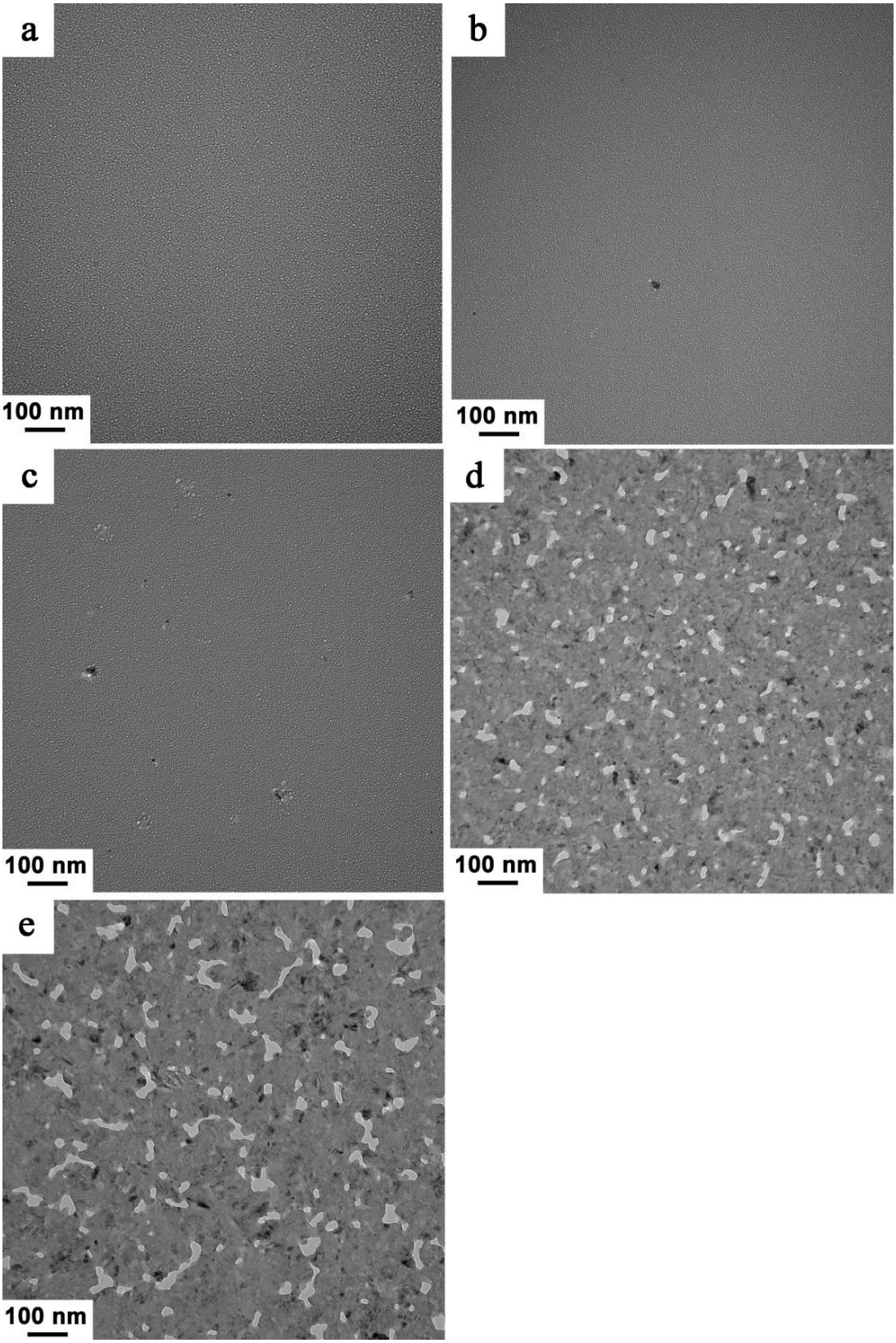

a
100 nm
b
100 nm
c
100 nm
d
100 nm
e
100 nm

Figure 5-5 TEM images of the OSO stacks annealed at 700 ℃ for (a) 1s, (b) 5s, (c) 10s, (d) 30s and (e) 60s.

After the same heating process, however, the OSO stack shows a different results. Figure 5-5 shows the TEM images of the OSO stack annealed at 700 ℃ for different time durations. No crystal is observed in the silicon film after 1s annealing at 700 ℃. The silicon is still completely amorphous. When the annealing time increases to 5 seconds, very few silicon nanocrystals are formed. No obvious pores can be seen in the TEM image. In this stage, crystallization process is dominant by the incubation of the crystal nuclei. Very few crystalline nuclei reach to the critical size that allows them to survive as nanocrystals. Even after 10s annealing, the silicon nanocrystals are very sparse. A few pits adjacent to the nanocrystals can be seen in the TEM image. The majority of the silicon film is still amorphous. After annealing for 30 seconds, the silicon film is pretty much crystallized and pores appear throughout the silicon film. Some smaller pores have a circular shape while the shape of the larger pores is mostly irregular. The size of nanopores grows even bigger when the annealing time increases to 60s. Some of these pores become more elongated and very irregular reminiscent of the coalescence of multiple-pores. This trend is in agreement with what we observed in the NSN stacks.

By comparing the annealing results from the NSN and OSO stacks, some differences appear. The first and foremost one is that the crystallization kinetics is different in these two stacks. Crystallization starts quite earlier in the NSN stack. The incubation of the silicon nuclei takes place occurring the temperature ramping up stage and the nucleation

starts immediately when the temperature reaches 700℃ in the NSN stack. However, no clear nucleation is observed in the OSO stack with the same heating process. In other words, even though the silicon films are of the same thickness, the crystallization speed of the silicon film is faster when sandwiched by the nitride capping layers than by the oxide layers. This indicates that the silicon crystallization is enhanced in the silicon film in the NSN stack compared to that in the OSO stack, which is probably due to the interface energy difference between silicon/silicon nitride and silicon/silicon dioxide [86-89]. Another difference is that pore density and porosity from the NSN stack are obviously larger than those from the OSO stacks, which is in consistent with the previous results in chapter 4. Since pore formation is directly associated to the silicon crystallization, it is more likely the enhanced silicon crystallization in the NSN stack helps to promote pore formation.

5.4 Multi-step Heating Process Study

The ex-situ heating study, described with previous section indicates that the crystallization enhancement in the NSN stack may be attributed to the promoted pore formation in the silicon film. Multiple-step heating experiment is conducted.

It is well known that silicon crystallization can be divided into two stages. The first one is the nucleation of silicon nuclei. In this stage crystal nuclei, known as ordered silicon atom clusters, start to form in the amorphous silicon matrix upon heating slightly below the crystallization temperature. When these silicon nuclei reach a critical size, the second stage of crystallization namely crystal growth starts. In this stage, silicon crystals keep

growing until they impinge with other crystals during the heating. As the heating goes on, silicon atoms in the amorphous phase add to the nanocrystals until the silicon film is fully crystallized.

In out multi-step heating experiment, we first heat the OSO sample slightly below the crystallization temperature to introduce crystal nuclei clusters in the amorphous silicon film. Then the temperature is increased above the crystallization temperature during a second-step to crystallize the amorphous silicon completely. With the two-step heating procedures we expect to achieve large nanocrystals since the crystal nuclei produced during the first heating step can directly grow into silicon crystals without nucleation initiation.

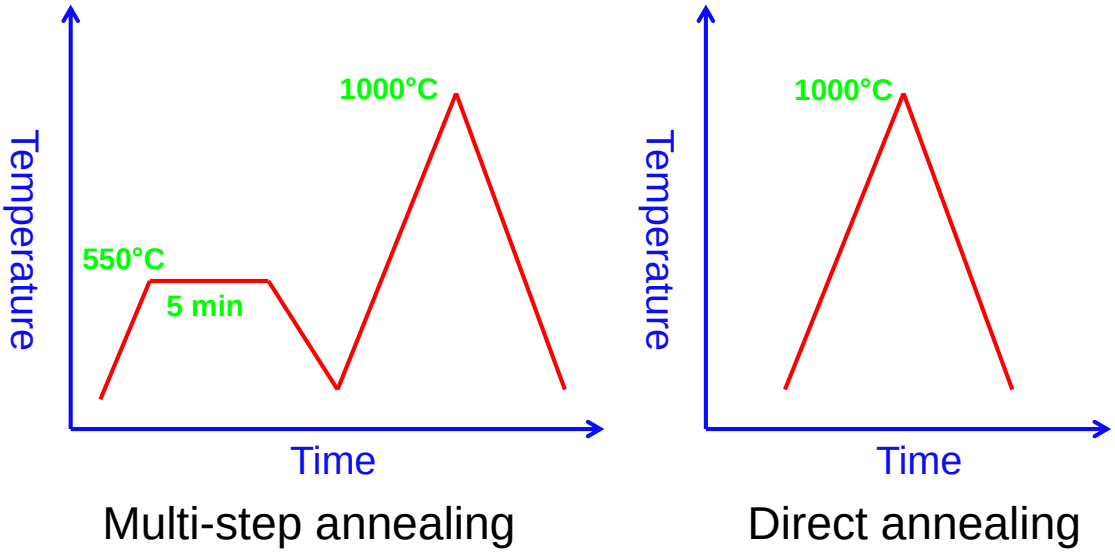


Figure 5-6 Schematic illustration of the multi-step and direct heating process.

The OSO stack with 15nm silicon films and 20nm oxide capping layers is used in this experiment. In the multi-step heating process, the temperature first set to 550 ℃ with a

50 ℃ /s ramp rate and then stays at constant for 5 minutes. After cooling down, the sample is subjected to a second-step heating process in which the sample is heated to 1000 ℃ with the same ramp rate and cools down right after the temperature reaches to 1000 ℃ (see figure 5-6). For the direct annealing, control sample is just going through the same heating process as the second step of the multi-heating process.

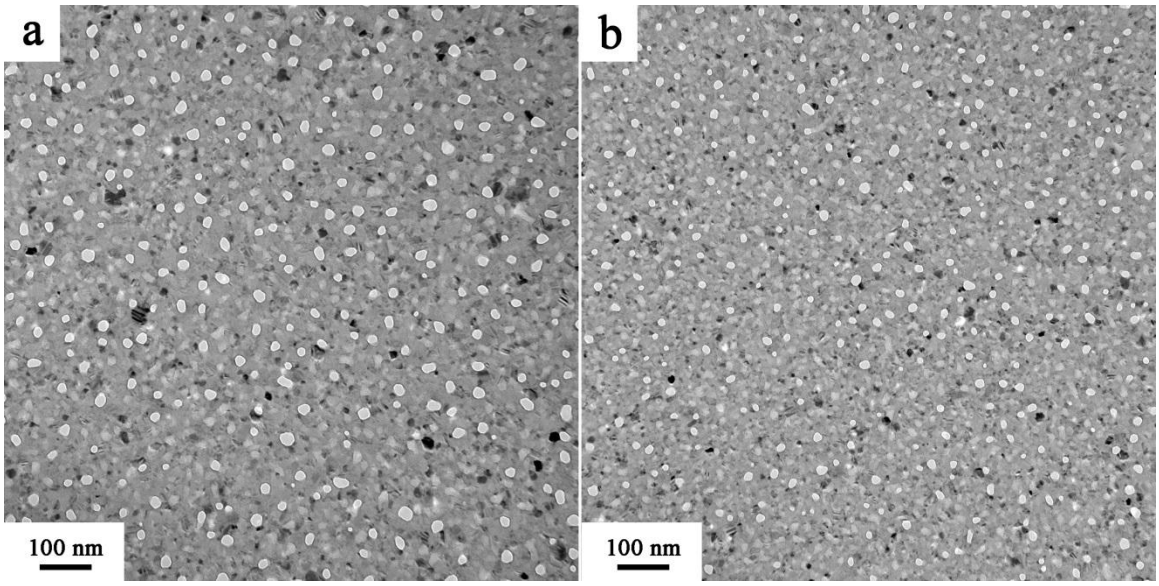


Figure 5-7 TEM images of the OSO stacks after (a) multi-step heating and (b) direct heating.

Figure 5-7 shows TEM pictures after the two different heating processes. It is clear that the multi-step heating process produces larger silicon crystals and bigger pores, consistent with our hypothesis. Pore characteristics comparison in figure 5-8 clearly shows that both the porosity and APD from the multi-heating sample are greater than those from the direct heating sample. The pore density plot, however, shows that the sample with single heating process produces a slight higher pore density than the multi-heating sample. The pore distribution plot reveals that majority pores from the single heating sample are

quite small with diameters from 10nm to 16nm. Sample with multi-heating treatment produces relative larger pores and majority of these pores are between 16nm and 22nm.

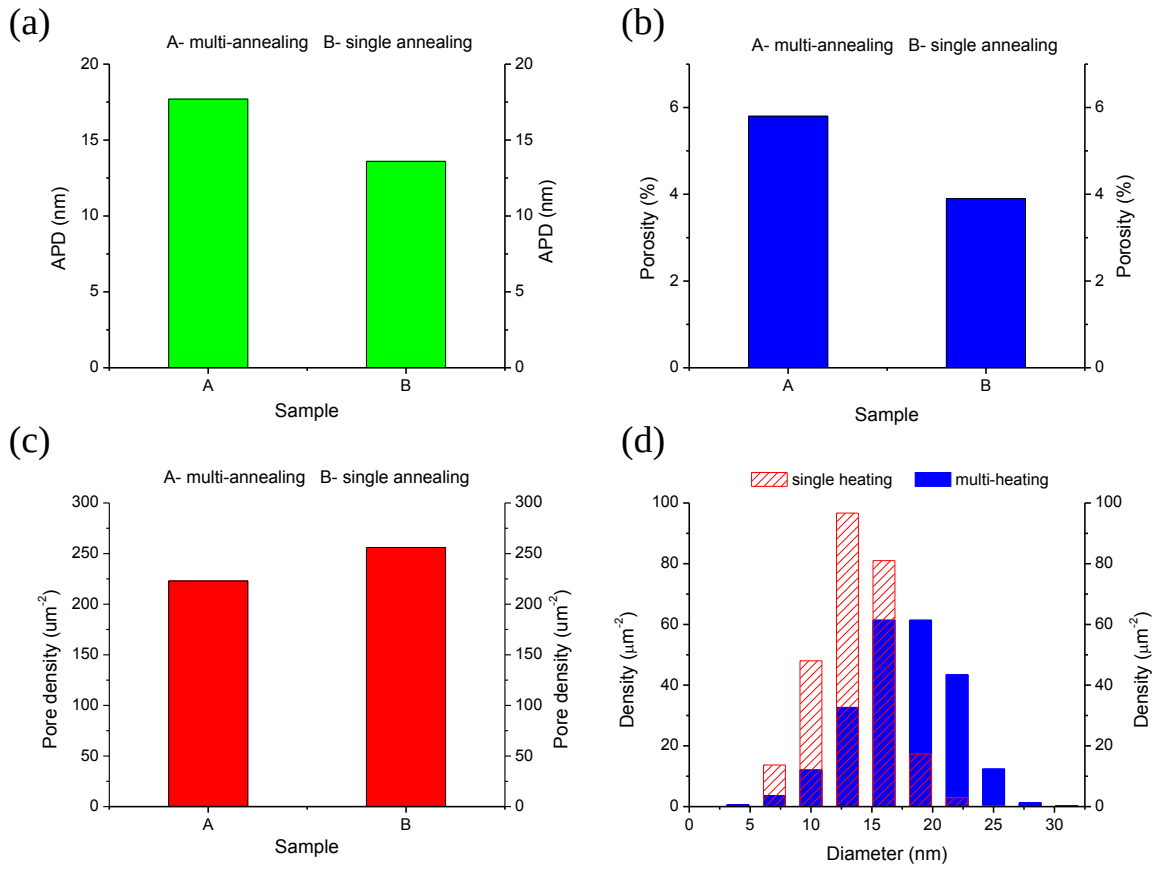


Figure 5-8 Pore characteristics comparison of the OSO samples with different annealing processes, (a) APD, (b) porosity, (c) pore density and (d) pore size distribution.

This multi-heating experiment demonstrates that pore formation and growth is strongly affected by the crystallization process of the silicon film. Multi-heating treatment enhances the silicon crystallization by introducing silicon crystal nuclei during the first-step low temperature heating and these crystal nuclei grow quickly to silicon crystals during the second-step high temperature heating process. Meantime, pores are associated

with the formation of silicon nanocrystals. Their sizes increase with the growth of silicon nanocrystals due to the diffusion of silicon atoms. This mechanism will be discussed in details in the following in-situ heating section.

5.5 In-situ Heating Study of Pore Formation

It is important to understand the silicon crystallization dynamics and kinetics in order to study the pore formation since it is associated with the phase transformation of the silicon film. In-situ TEM has been a useful tool to capture the dynamical crystallization information and provide insights of the phase transformation process.

5.5.1 Sample Preparation

A TEM heating holder (Gatan Single Tilt Heating Holder 628) is used to conduct the in-situ heating experiments in FEI Osiris TEM. Figure 5-9 shows the photographs of the heating holder and the FEI Osiris TEM. This heating holder is a furnace-type holder made from tantalum that can be heated up to 1300 ℃. Samples are placed in the furnace between two washers and are tightened with the Hexring clamp.

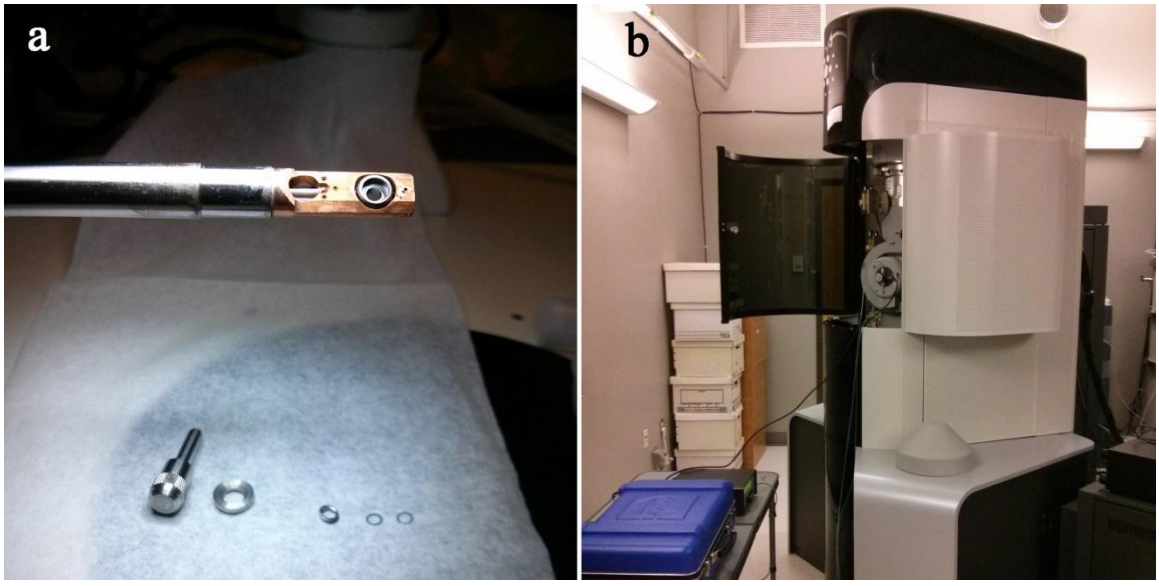


Figure 5-9 Photographs of (a) Gatan 628 single tilt heating holder, and (b) FEI Osiris TEM.

The sample preparation process for in-situ heating experiments is illustrated in figure 5-10 (a). Silicon wafers are first patterned with TEM grid designs using standard lithography technique. Three-stack structure either the OSO or NSN is then sputtered on the non-patterned side of the silicon wafer. After deposition, silicon wafers is going through a wet etching process from the pattern side to remove the silicon substrate and expose the free-standing three-layer stack for in-situ heating study.

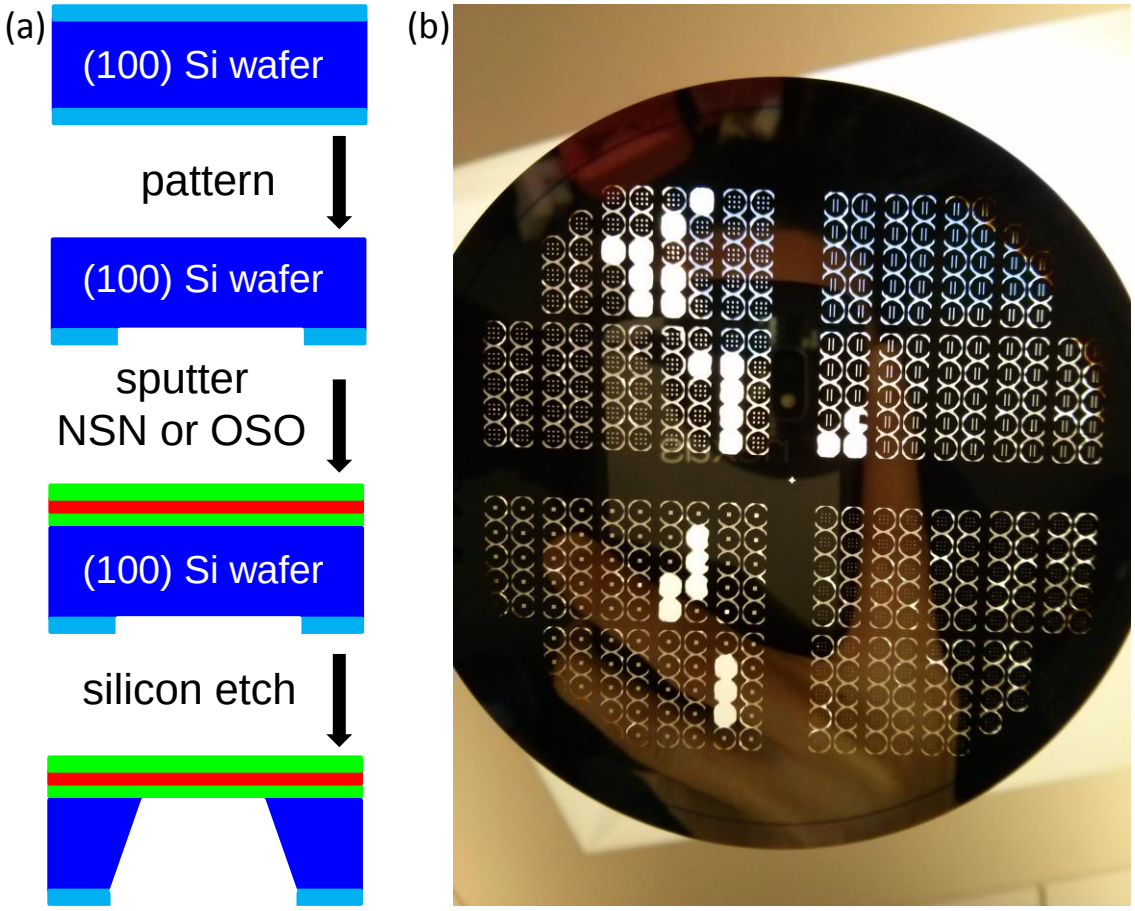


Figure 5-10 (a) Illustration of sample preparation process and (b) photograph of membrane TEM grids with different patterns.

Figure 5-10 (b) shows a photograph of the TEM grids with different patterns. The free-standing membranes are so thin that light can directly pass through and that is why membranes look like transparent under light. Each TEM grid is easy to pop out from silicon wafer and can be used for in-situ heating experiment.

5.5.2 In-situ Heating of the OSO Stack

To investigate the pore formation details during heating process, in-situ heating of the OSO stack is conducted using the TEM heating holder. The thickness of the silicon film is 15nm and the top and bottom oxide layers are 10nm and 20nm respectively. Sample is heated inside the TEM chamber and auto recording function is applied to record image every 2.5s automatically. These recorded images can later be used to create in-situ heating videos.

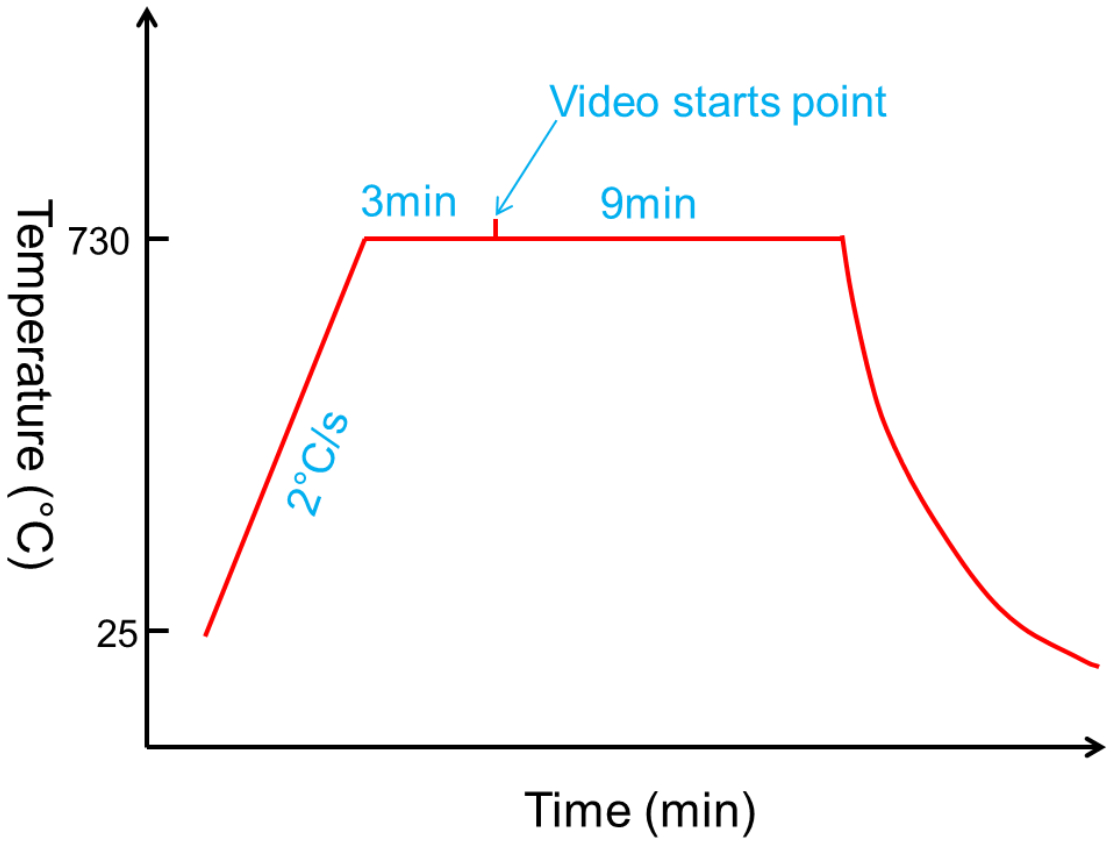
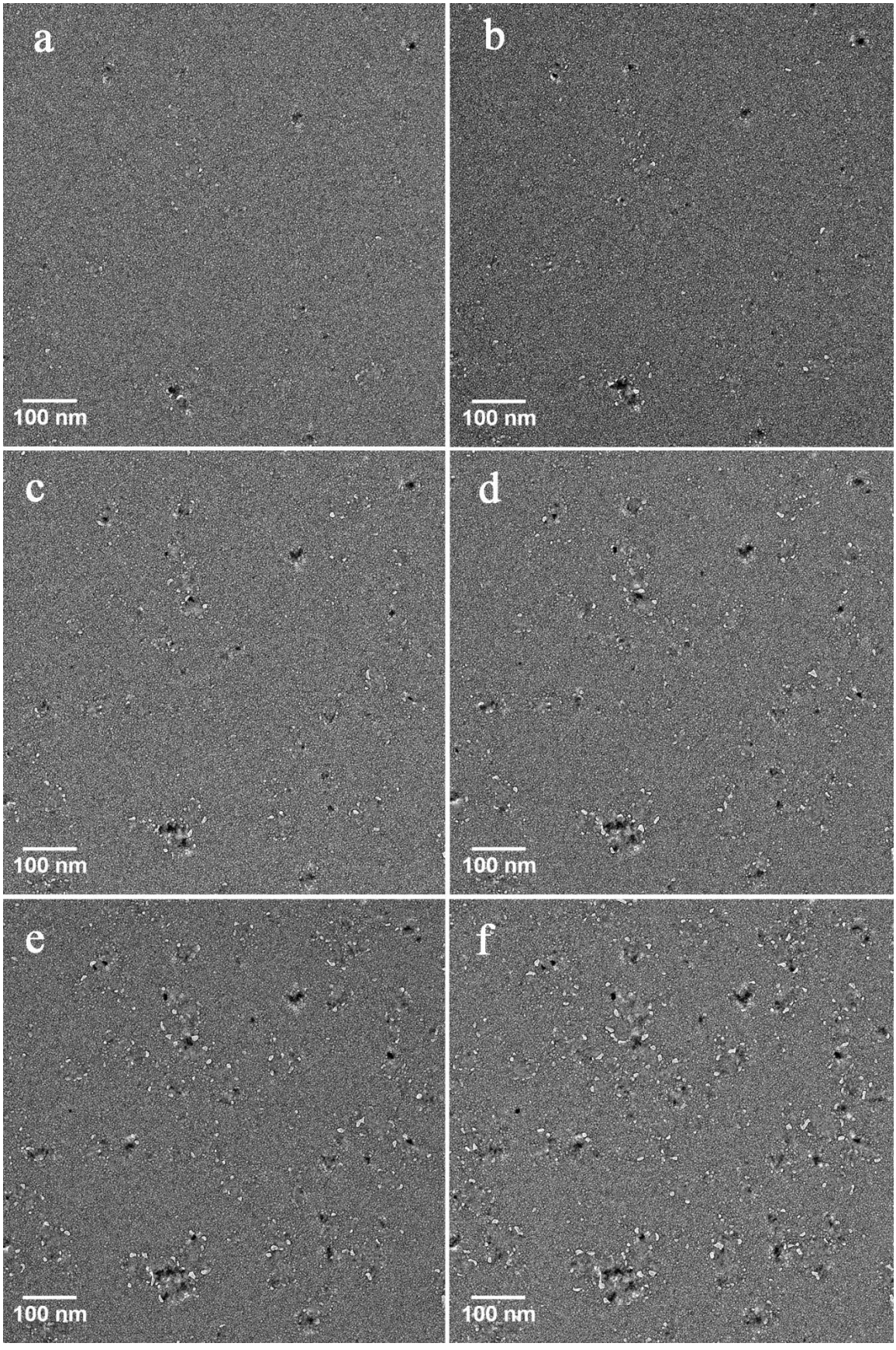


Figure 5-11 Illustration of the in-situ heating process for the OSO201510 sample.

Figure 5-11 illustrates the heating process for the OSO sample. This sample is first heated up to 730 ℃ with a slow ramp rate of 2 ℃/s. The reason to use a slow ramp rate is

to reduce sample drifting for better imaging process. It has been found that higher ramp rate results in very severe sample drifting, which makes image recording very difficult. The auto recording function is applied to record the crystallization and pore formation process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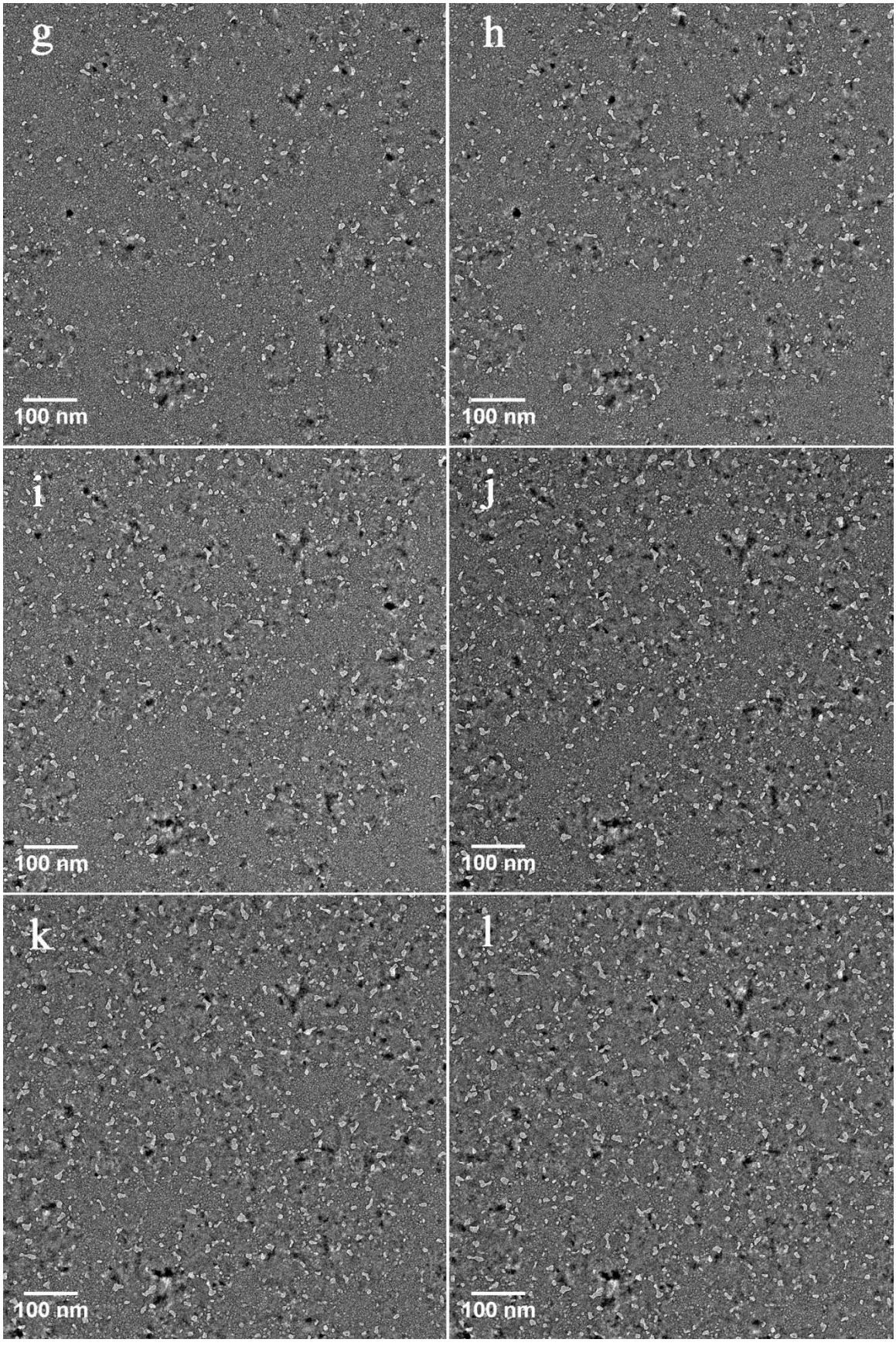
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Figure 5-12 TEM images of in-situ annealing of the OSO sample at 730℃ for successive time; the time interval between each image is 25s.

Figure 5-12 shows the dynamical process of silicon crystallization and pore formation in the OSO stack during in-situ heating process. The formation of silicon nanocrystals is observed after the sample is heated at 730℃ for 3 minutes. Pits and voids that are surrounding the Si nanocrystals are formed at the same time. In other words, the silicon nucleation and nuclei growth involve the rearrangement of Si atoms, which results in formation of pits and voids that surround the Si nanocrystals.

As the heating process continues, Si nanocrystals keep growing in lateral directions since they are confined in the thickness direction. Meanwhile, pits and voids continue growing as more and more silicon atoms move to silicon nanocrystals to keep crystal growth. As a result, these pits easily span over the silicon film in thickness direction to form pores since the silicon film is only 15nm thick. As the growth of silicon nanocrystals keeps going, pores are moving from the amorphous/crystalline interface towards the amorphous matrix. It seems that pores movement facilitates the Si crystallization. In fact silicon nanocrystals attract the nearby Si atoms from amorphous matrix to keep the growth of the ordered crystal structure, which results in the pores movement. The crystallization process is complete with the sign of no more new pore forming or pore movement because most of the amorphous silicon is transformed into crystalline phase.

5.5.3 In-situ Heating of the NSN Stack

The heating process for the NSN stack is similar as the previous one for the OSO sample. The silicon film is 15nm and the nitride capping layers are 30nm in this NSN stack. This sample is heated to 730 ℃ with 2 ℃/s ramp rate. After holding at the set temperature for a couple of minutes, crystallization and pore formation are observed and the auto recording function is turned on to record the dynamical crystallization process. Figure 5-13 illustrates the heating process of this sample.

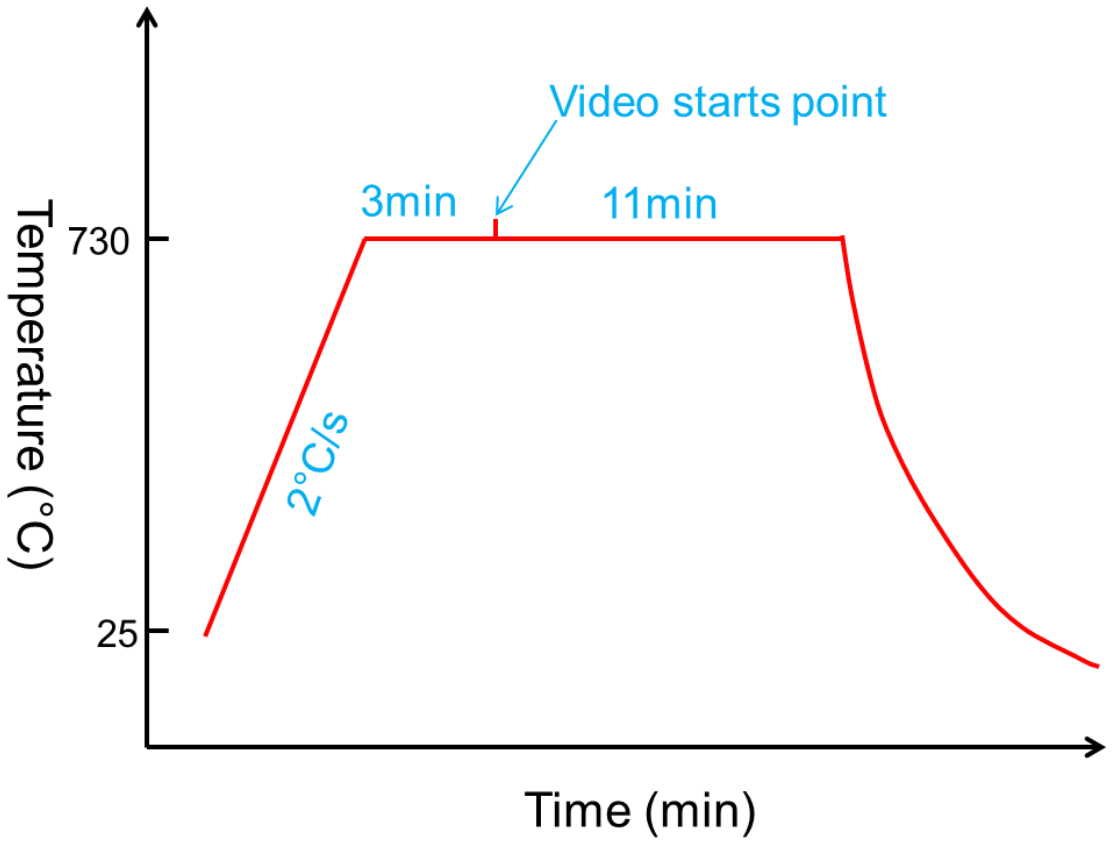
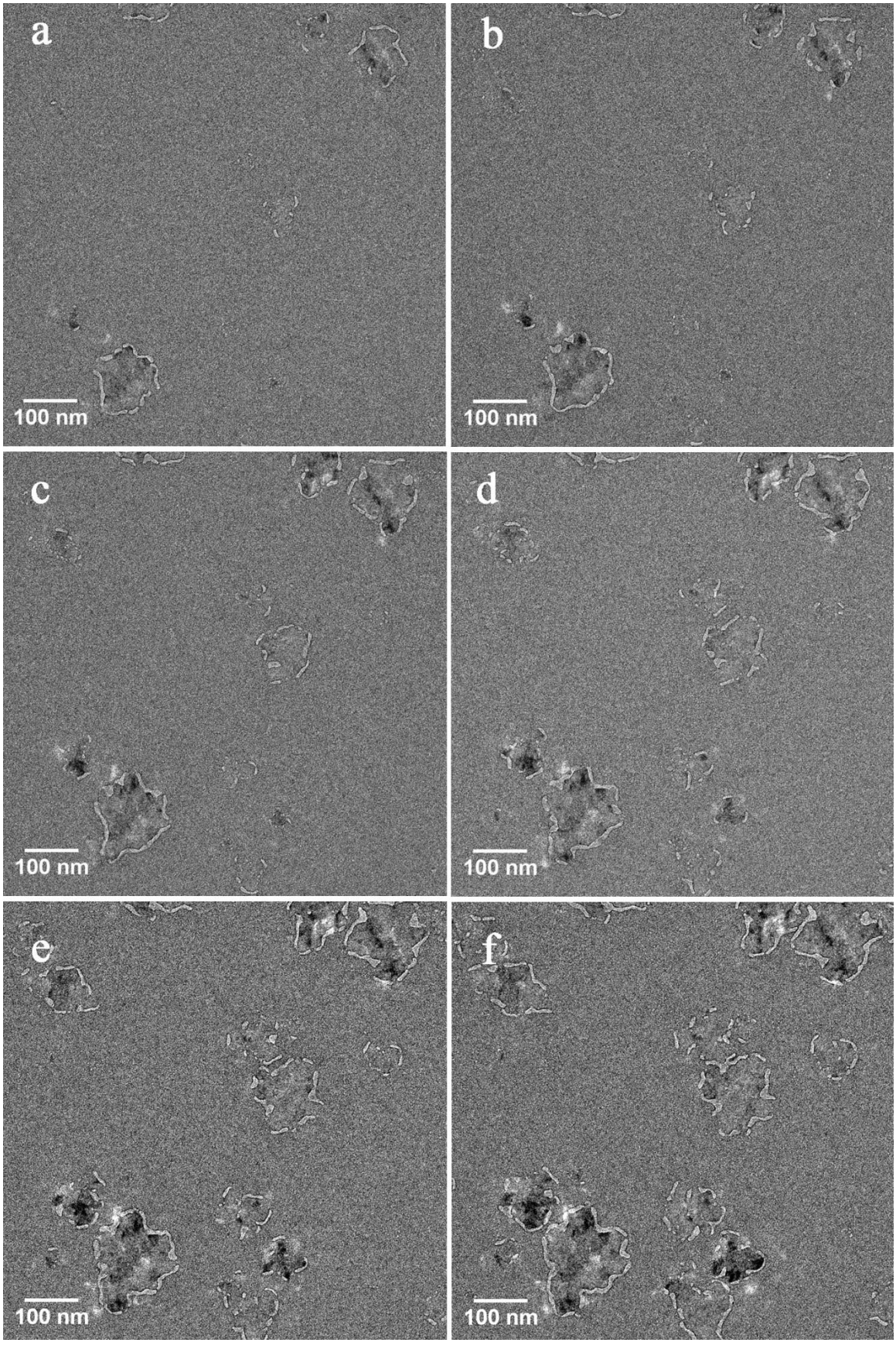


Figure 5-13 Illustration of the in-situ heating process for the OSO201510 sample.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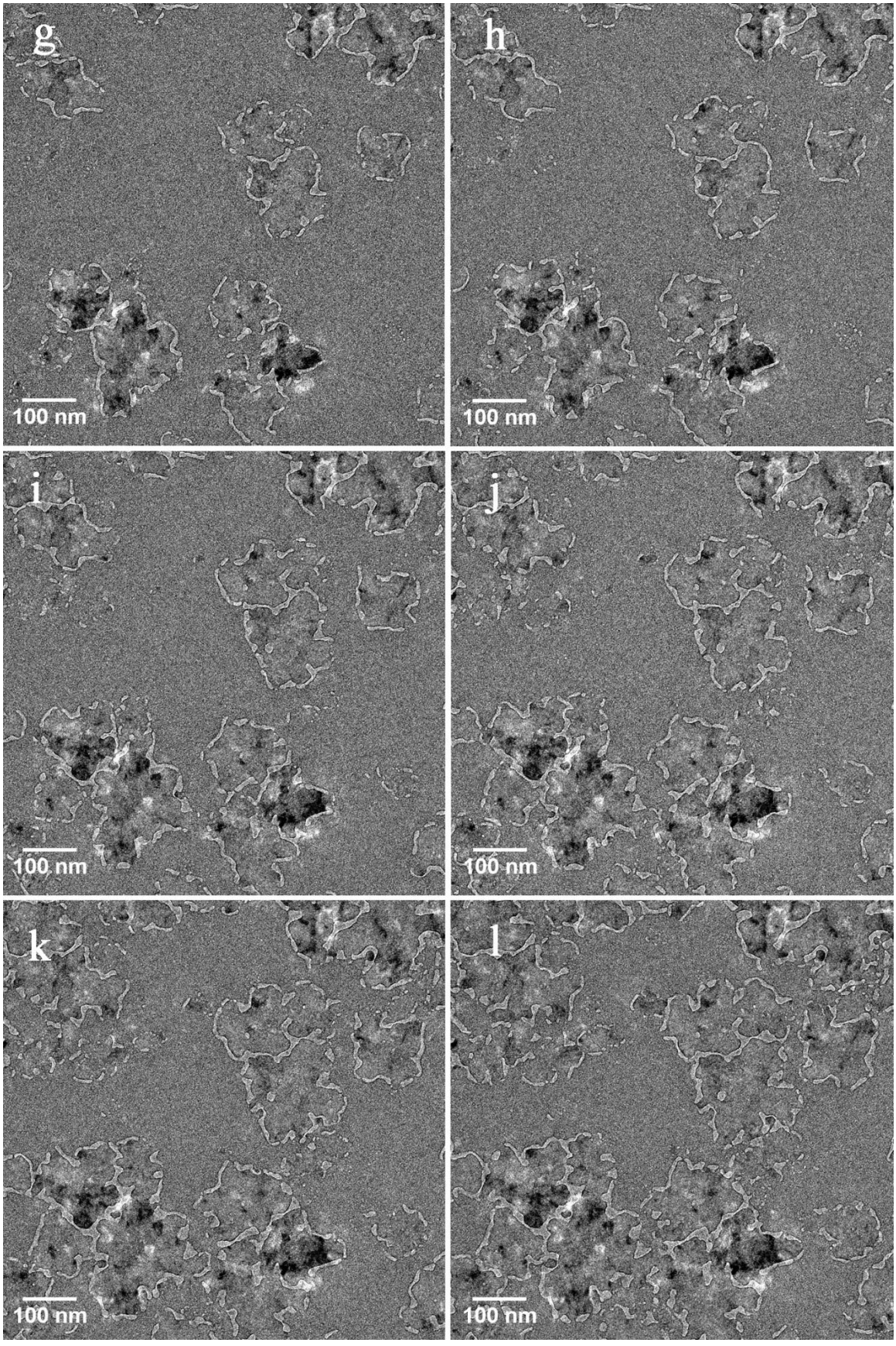
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Figure 5-14 TEM images of in-situ annealing of the NSN sample at 730℃ for successive time; the time interval between each image is 25s.

Silicon crystallization and pore formation are clearly observed in this NSN sample during in-situ heating process (figure 5-14). However, Si crystallization and pore growing in the NSN stack behave very differently compared to that in the OSO sample. Crystallization is accompanied with the surrounded pit formation. These surrounded pits grow to pores with the growth of silicon nanocrystals. An interesting pattern is form by these pores and we name it 'pearl necklace' pattern. The 'pearl necklace' pattern is referred to that pores look like pearls in white and they form a circular pattern that surround silicon nanocrystals like a necklace shape. These pearl necklace patterns behave like the interface of the amorphous silicon and crystalline silicon. They grow bigger in diameter and expand to the amorphous region with the continuation of the crystallization process. As these pearl necklace patterns grow bigger, they start losing the circular shapes by the means of either pore segmentation or pore coalescence, especially when these pearl necklace patterns grow to each other. Due to more pores merge and coalesce with adjacent ones as they move in the amorphous silicon, their shapes become very elongated and flexuous. Pore movement stops when the surrounded amorphous silicon has fully transformed to crystalline phase. As a result, these pores end up with elongated and irregular shapes after the annealing.

Apparently the NSN stack shows a very different pore growing pattern compared to the OSO stack. In the NSN stack, since the voids form so readily and maintain the ring so well, it restricts the flow of silicon atoms into the growing crystal, slowing things down,

and allowing the ring of void to grow in a stable manner. However, in the OSO stack, the voids seem to be smaller and less defined, and do not seem as free to move outward as the central crystalline area grows. This appears to allow the crystal to be less confined by the void and be fed much more readily by the surrounding silicon atoms. As the crystalline fingers race past and through the void ring, individual voids are forced not only outward, but also laterally, creating all the complex paths. This difference in pore growth pattern in the NSN and OSO stack eventually results in the different pore characteristics such as pore size, shape and porosity.

5.6 EDS Mapping Study of Pores

FEI Tecnai Osiris offers high speed and high sensitivity energy dispersive X-ray spectroscopy (EDS) mapping capability for materials analysis. The high angle annular dark field (HAADF) imaging operated in scanning transmission electron microscopy (STEM) mode is very powerful to study pores in pnc-Si membranes by providing useful tomography information from the STEM images. Both the NSN and OSO stacks are systematically studied with STEM and EDS mapping in the following sections.

5.6.1 EDS study of pores in the NSN stack

The EDS technique is used to analyze the elements in the NSN stack. Figure 5-15 shows the EDS spectrum of the pre-annealing NSN stack. This stack is made of 25nm silicon film sandwiched by 30nm silicon nitride capping layers. Major peaks including silicon, nitrogen and oxygen are displayed in the spectrum, which belong to the NSN

sample. The aluminum peak is from the TEM sample clip. An interesting element, argon, is found in the NSN sample. This is not surprising since Ar is the source gas for sputtering process and it is common that some Ar molecules embed into deposited films during the deposition.

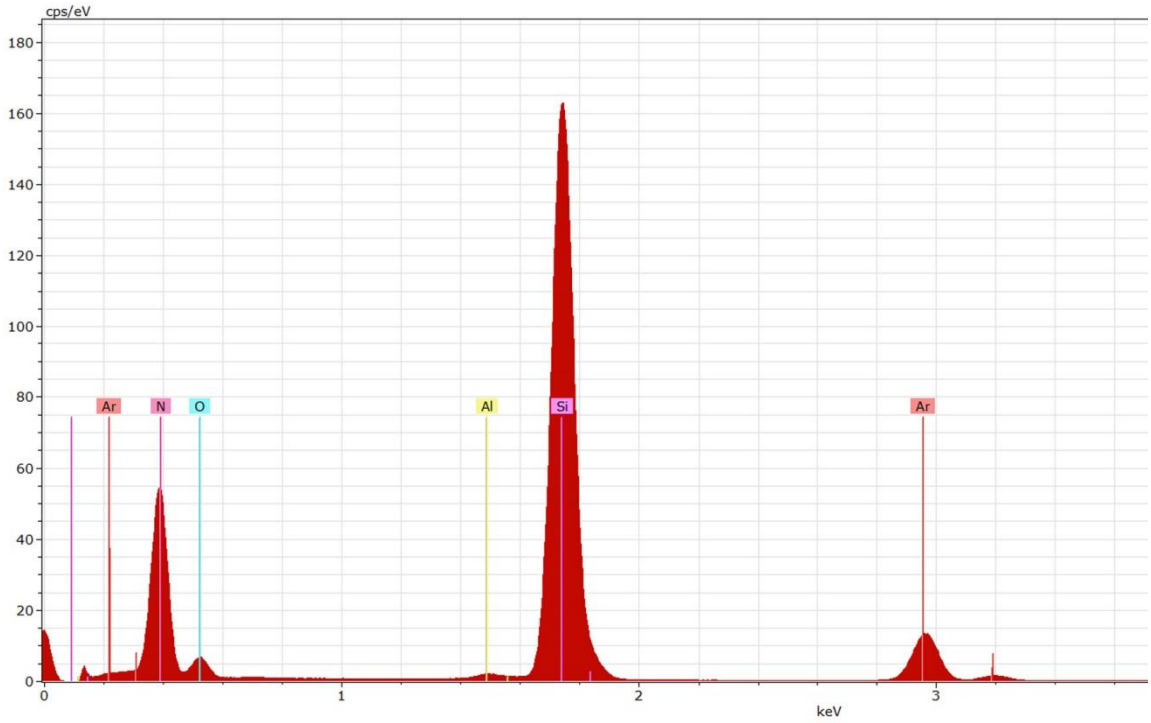

Figure 5-15 EDS spectrum of the pre-annealing NSN stack.

Table 5-1 shows compositions of the interested elements calculated from the EDS spectrum. Silicon element is around 60% and nitrogen holds around 33% in atomic percentage. Surprisingly Ar occupies 4.8% atomic percentage, which is relatively high.

Table 5-1 Elemental compositions of the pre-annealing NSN stack.

Element	[wt.%]	[norm. wt.%]	[norm. at.%]	Error in wt.% (3 Sigma)
Silicon	70.66	70.66	59.63	0.19
Nitrogen	19.48	19.48	32.96	1.83
Argon	8.11	8.11	4.81	0.81
Oxygen	1.76	1.76	2.61	0.23

STEM mapping result of the amorphous NSN is shown in figure 5-16. It shows silicon element is evenly distributed and shows featureless characteristic, which is in consistent with the amorphous nature. Argon and nitrogen elements mapping results look very similar as to that of the silicon element because they are also evenly distributed in the NSN stack.

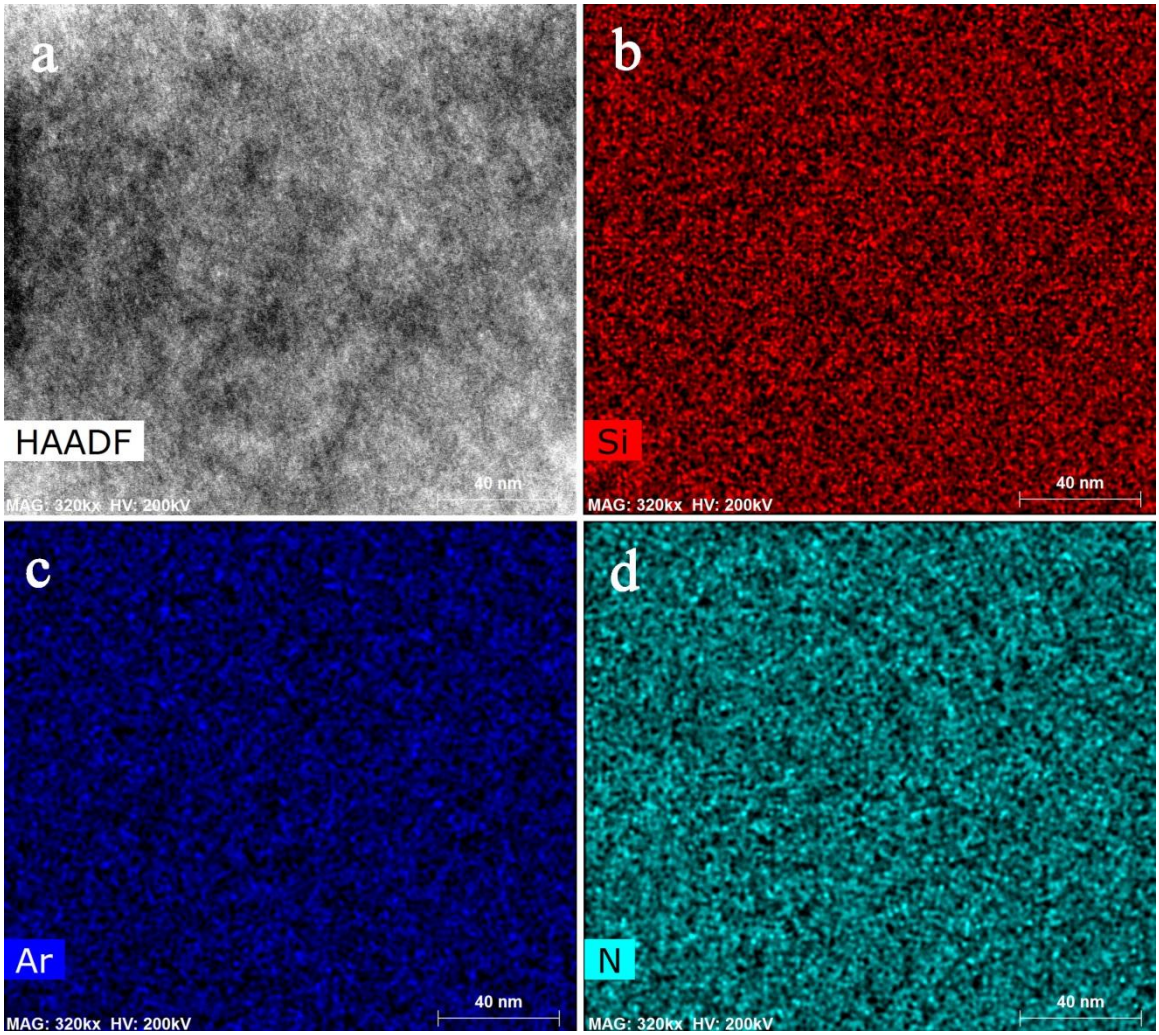

Figure 5-16 EDS mapping results of the amorphous NSN stack, (a) HAADF image, (b) Si, (c) Ar, and (d) N.

This sample is heated to 750 ℃ to introduce silicon crystallization and pore formation in the silicon film. We use EDS mapping to map the element distribution in this sample after annealing. A very interesting mapping result is shown in figure 5-17. In HAADF image pores are showing in black and silicon crystals in white, which is the opposite of bright field image. Pores are also showing in black areas Si mapping result because less or

no silicon single could be acquired from these regions. Ar, however, seems to concentrate in those holes in the silicon film in the mapping result. This is the first time we noticed that Ar occupies these pores in the silicon film. It indicates that embedded Ar molecules are also involved in the silicon crystallization and pore formation in the heating process. A possible explanation is that during heating process these embedded Ar molecules have enough mobility to move around and precipitate with other Ar molecules, which ends up forming bubbles. These small Ar bubbles grow bigger as more Ar molecules diffuse in. As a result, pits and voids are formed in the silicon film due to these Ar bubbles. In addition, these bubbles coalesce or split as the crystallization process keeps going. Eventually they stop moving due to the completion of crystallization and are trapped in these pores. It seems that Ar molecules play a big role in silicon crystallization and pore formation process. People [90-92] have done research on the influence of noble gas on the recrystallization of implanted amorphous silicon. Revesz *et al.* [91] studied the epitaxial regrowth of Ar-implanted amorphous silicon and their result demonstrated the formation of Ar bubbles during implantation and the growth of these Ar bubbles during epitaxial regrowth of the amorphous silicon upon annealing process.

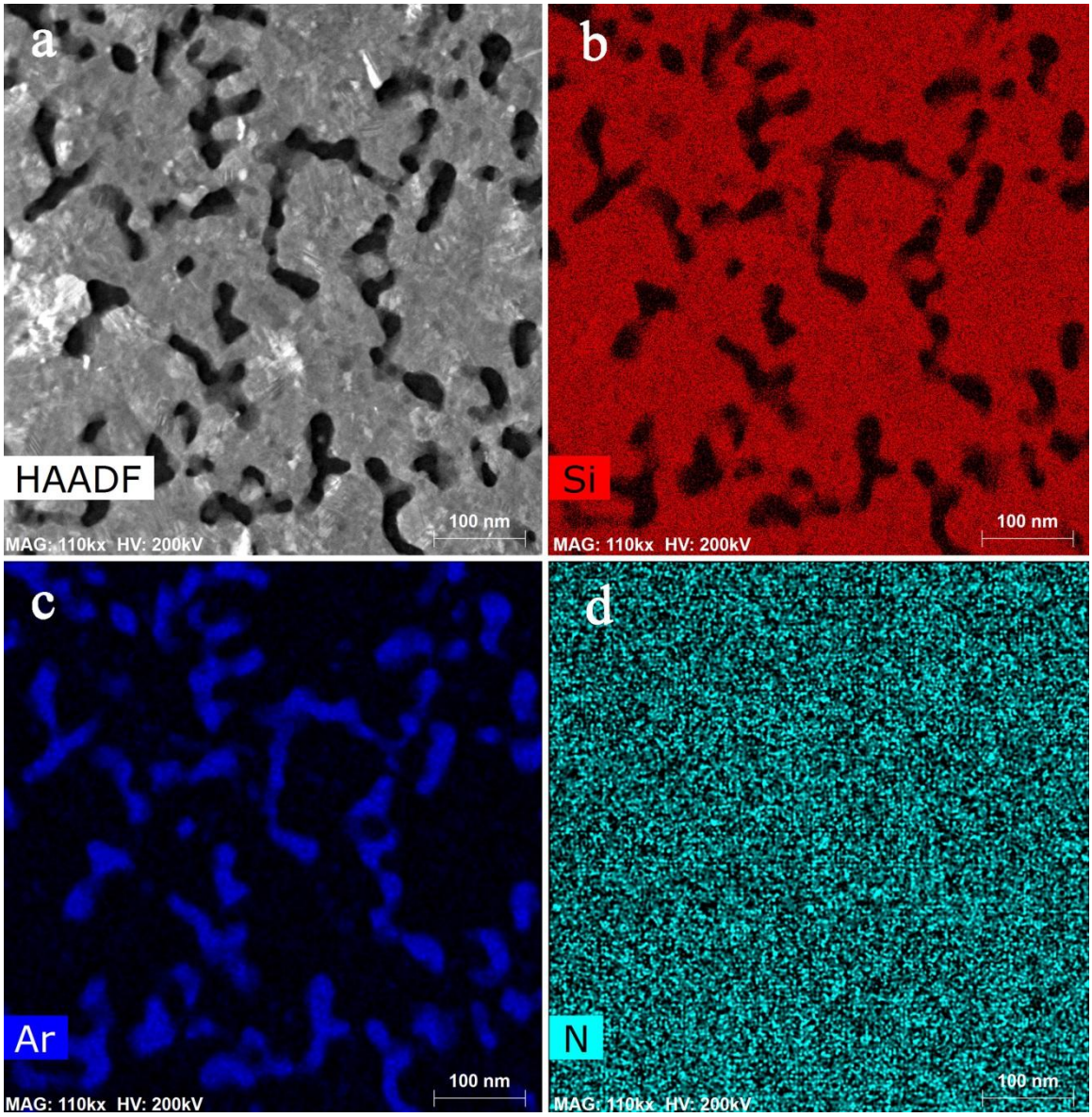

Figure 5-17 EDS mapping results of the annealed NSN stack with nitride capping layers, (a) HAADF image, (b) Si, (c) Ar, and (d) N.

To verify the gaseous phase of Ar bubbles, the capping silicon nitride layers are removed to see whether these Ar bubbles could escape. Figure 5-18 shows the EDS spectrum of the annealed NSN stack with capping nitride layers removed. It can be clearly

seen that both the nitrogen and argon peaks are gone in the spectrum. Silicon peak becomes the major one in the spectrum. Two tiny peaks including oxygen and carbon are believed from the oxidation and contamination during the etching process. It confirms that Ar in the porous areas is in gaseous phase and this explains why no Ar peak shows up in the EDS spectrum after removing the protective nitride layers. The silicon nitride capping layers prevent Ar bubbles escaping from porous areas in the silicon film.

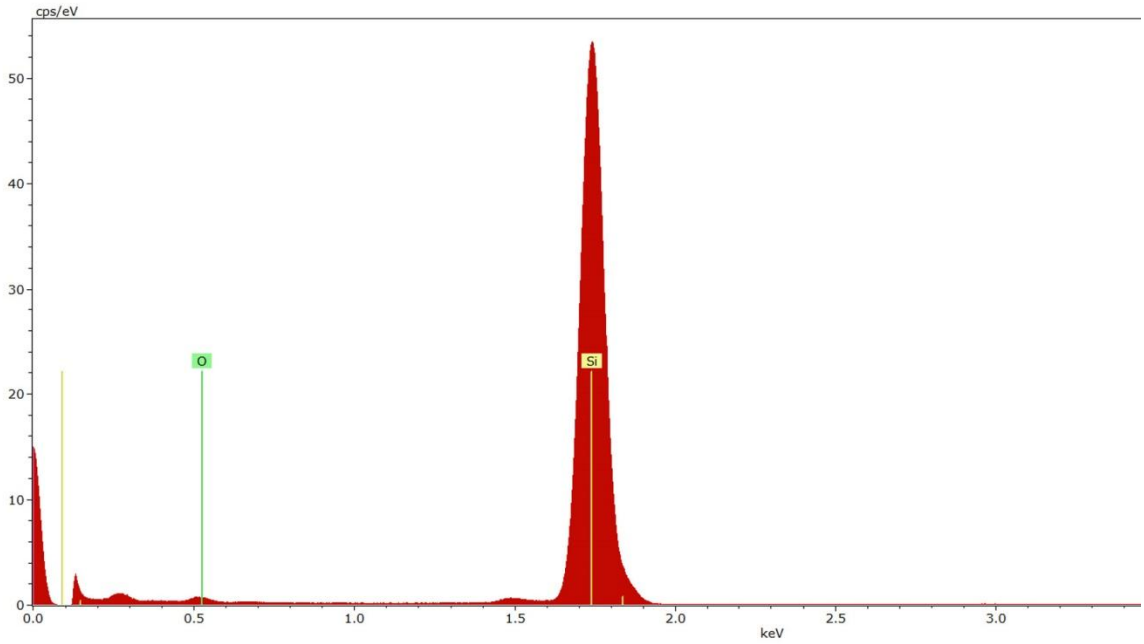

Figure 5-18 EDS spectrum of the annealed NSN stack with nitride removed.

5.6.2 EDS study of pores in the OSO stack

The NSN stack demonstrates a very intriguing result of highly concentrated Ar bubbles in pores in the silicon film after annealing. Since the OSO stack shows different crystallization and pore formation dynamics than the NSN stack, it is very interesting to

study the EDS mapping of the OSO stack. We select the OSO sample with the same thickness profile as to that of the NSN stack, which contains a 25nm amorphous silicon film with 30nm silicon dioxide capping layers.

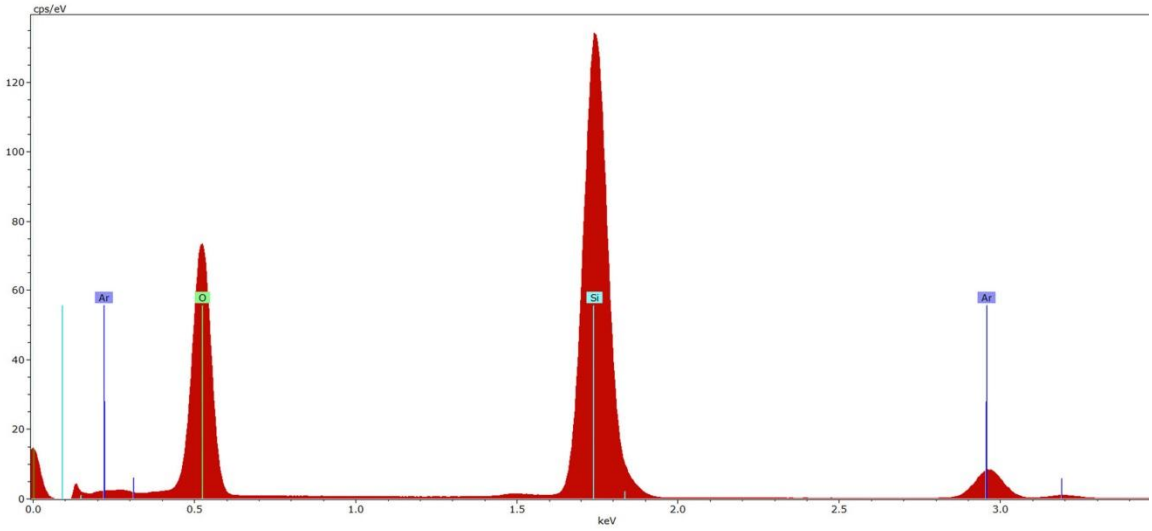

Figure 5-19 EDS spectrum of the pre-annealed OSO stack.

Figure 5-19 shows the EDS spectrum of the OSO stack before annealing. Besides Si and O elements, Ar is also detected in the EDS spectrum. The detected Ar is in agreement with previous result from the NSN stack since all the depositions are done with Ar plasma. Composition result is shown in table 5-2. The silicon element is dominant the whole stack with an atomic percentage of 57% and oxygen occupies another 39%. Argon takes part in about 3.5% atomic percentage in the whole sample. It is a little lower than that in the NSN stack, which is 4.8%. This could be due to the difference in deposition parameters, such as working pressure, which may affect the argon embedding. Silicon nitride films are deposited at 5mT working pressure where it is 3mT for silicon dioxide films.

Table 5-2 Elemental compositions of the pre-annealing OSO stack.

Element	[wt.%]	[norm. wt.%]	[norm. at.%]	Error in wt.% (3 Sigma)
Oxygen	26.33	26.33	39.12	2.45
Silicon	67.78	67.78	57.37	0.18
Argon	5.89	5.89	3.51	0.61

This OSO stack is going through a same annealing process to introduce silicon crystallization and pore formation in the silicon film. Figure 5-20 shows the EDS spectrum result of this annealed OSO stack with the capping oxide layers. Surprisingly no Ar peak is detected in the EDS spectrum. Only Si and O peaks are observed. This means that Ar molecules escape from the OSO stack during the annealing process even though they are capped by silicon dioxide layers. In other words, Ar molecules diffuse out of silicon dioxide films during annealing process.

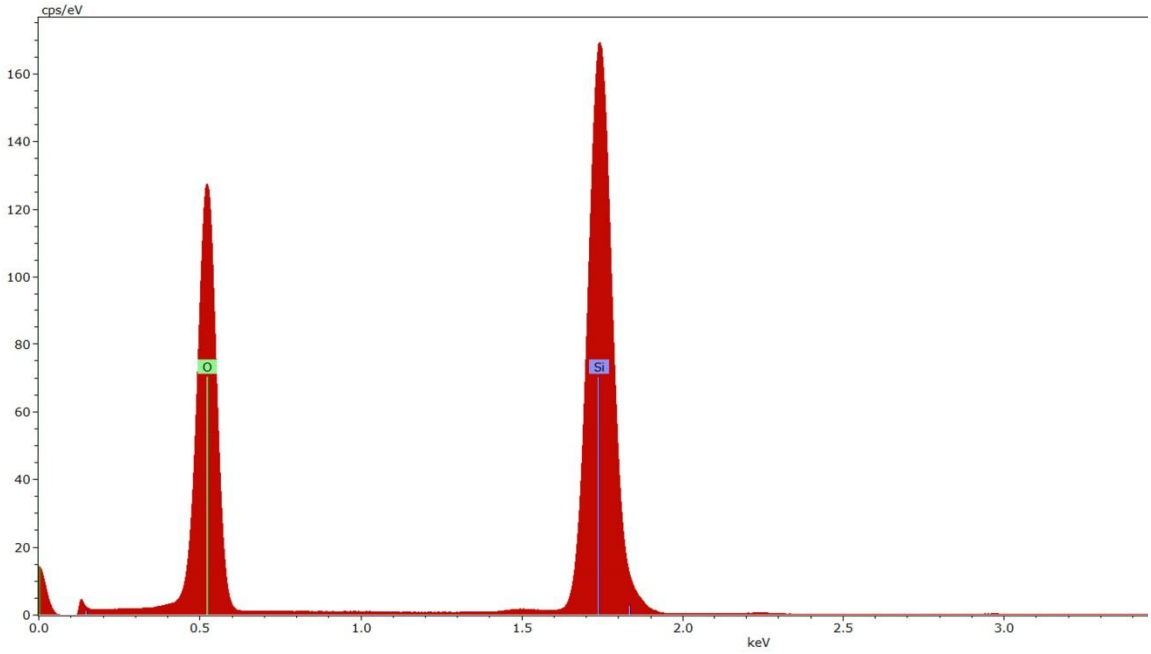

Figure 5-20 EDS spectrum of the annealed OSO stack.

EDS mapping is conducted to map the elements in the OSO sample. Figure 5-21 shows the mapping result of this sample. No Ar element can be detected and only Si and O elements are mapped. The Si element mapping result is consistent with the HAADF image where pores are shown as black areas because of less or no silicon signals. The O element covers the whole mapping area due to the capping oxide layers. This mapping result further confirms that the embedded Ar molecules escape from the OSO stack by diffusion during the heating process.

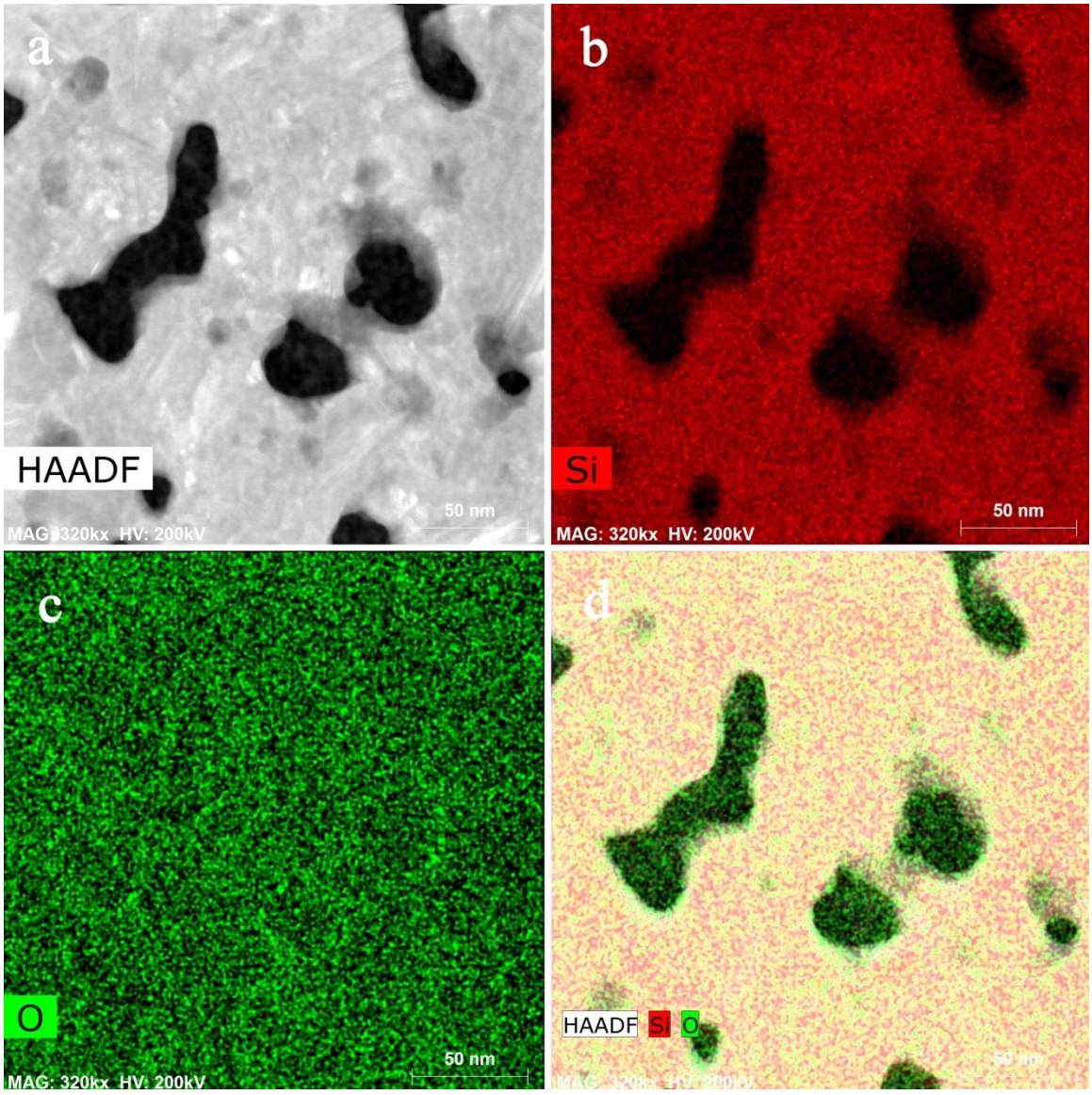

Figure 5-21 EDS mapping results of the OSO stack after annealing at 1000 ℃, (a) HAADF image, (b) Si element, (c) O element and (d) integrated mapping results.

By comparing the mapping results of the annealed NSN and OSO stacks, it shows that Ar molecules behave differently in the pore formation process during annealing process in both stacks. Silicon nitride capping layers keep Ar bubbles in porous area from

diffusing out during silicon crystallization process while Ar molecules escape from the silicon film when capped with oxide layers. This may explain the different pore growth patterns in the NSN and OSO stacks.

5.7 Pore Formation Process

Pore formation process in the pnc-Si membrane is thermally driven and associated with crystallization of the silicon film. Since silicon crystallization can be separated into two stages, i.e. nucleation and growth, it is wise to understand the pore formation in two stages including void nucleation and pore growth. These two stages are closely affected by the heating process and will be discussed in the following subsections.

5.7.1 Void Nucleation

The silicon nanocrystal nucleation is critical to the process of void nucleation. It has been pointed out that the interface of amorphous silicon and silicon dioxide (a-Si/SiO_2) is the preferred site for SPC nucleation. [93] In the OSO stack, two amorphous silicon and silicon dioxide interfaces work as the heterogeneous nucleation centers during the SPC nucleation. Silicon nuclei are formed at the interface of amorphous silicon and silicon dioxide films during heating process. At the same time, nano-voids start forming in the silicon film as a result of silicon diffusion due to silicon nucleation. This can be understood by the illustration of figure 5-22.

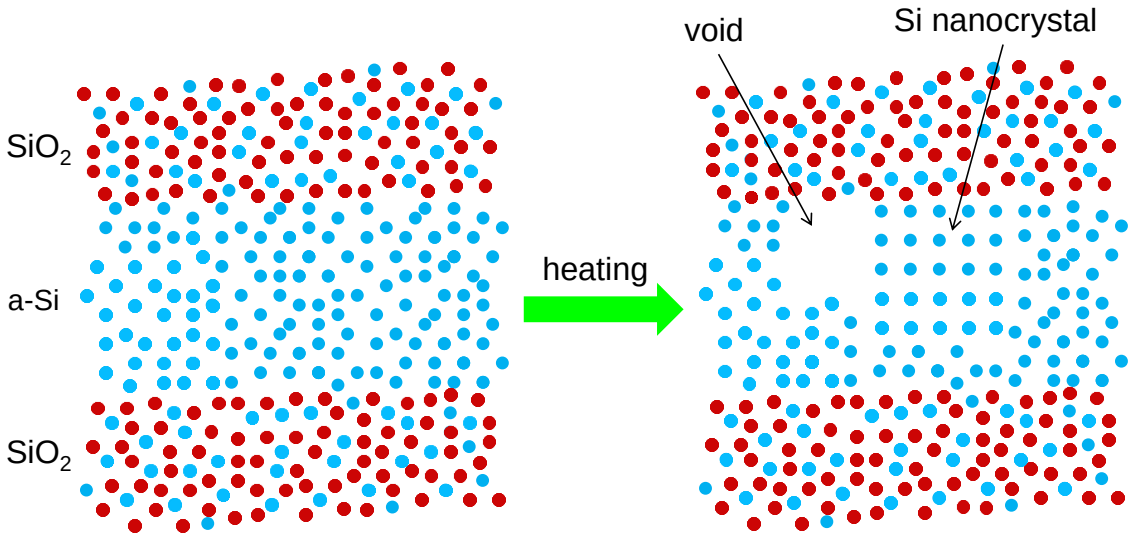

Figure 5-22 Illustration of void nucleation during the heating process. Cyan balls are silicon atoms and maroon balls are oxygen atoms.

As shown in figure 5-22, silicon nuclei are formed in the interface of silicon dioxide and amorphous silicon films during heating process. With the heating continues, more silicon atoms from the amorphous silicon matrix move to silicon nuclei and these nuclei grow to nanocrystals. As a result, vacancies are formed due to the left of silicon atoms and they eventually grow to nano-voids.

5.7.2 Pore growth

Pore growth is associated with the growth of silicon nanocrystals. With the heating process continues, the crystallization process keeps going accomplished by the crystal growth. This results in the formation of through pores in the silicon film, which is illustrated in figure 5-23.

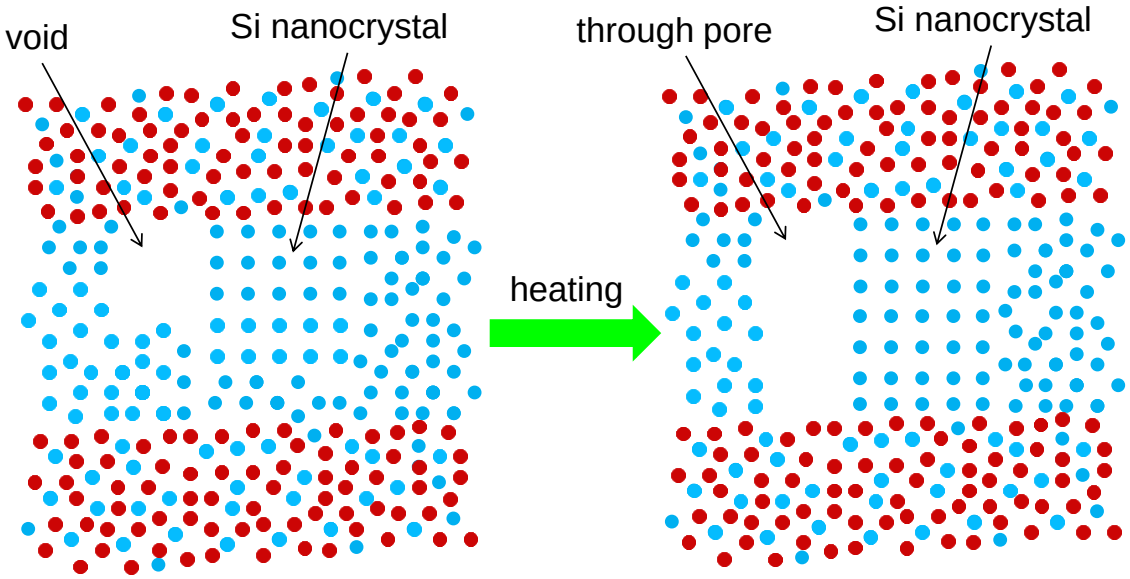

Figure 5-23 Illustration of pore growth during the heating process. Cyan balls are silicon atoms and maroon balls are oxygen atoms.

The size of silicon nanocrystals keeps growing until the amorphous silicon is fully crystallized as the heating process continues. This results in the growth of nano-voids in three-dimension due to the diffusion of silicon atoms. Since the amorphous silicon is confined in the thickness direction by two oxide capping layers, the growth of nano-voids spans the silicon film in the thickness direction and this leads to the formation of through pores, as illustrated in figure 5-23. Once through pores are formed, the growth of pores is achieved in the horizontal directions, which represents the diameter of pores. This process continues until the amorphous silicon is fully converted to a crystalline phase during the heating process.

The pore growth process is strongly affected by several factors such as silicon thickness, temperature ramp rate and capping layers. The thickness of the amorphous silicon film determines the freedom of void growth in the thickness direction. When the silicon film is very thin, for example 15nm, it is relative easy for nano-voids to span the entire silicon film to form through pores. The reason is because that the crystallized silicon film is a mono-layer of silicon nanocrystals. However, when the amorphous silicon is very thick, for example, greater than 100nm, very few through pores can be formed in the silicon film. This is due to the inhibition of voids growth in the thickness direction from the underneath or above nanocrystals. The mono-layer of nanocrystals in the silicon film is no longer true when the silicon film is very thick. Instead, a multi-layer of silicon crystals would be formed in the silicon film when the crystallization process is done. As a result, the growth of nano-voids at the interface of silicon and silicon dioxide films is limited by the underneath or above silicon nanocrystals, which results in pits and voids morphology. Figure 5-24 shows the cross-sectional SEM image of 100nm thick pnc-Si membranes after annealing. Nano-pits and voids, instead of through pores, are the dominant features in the cross-sectional silicon film.

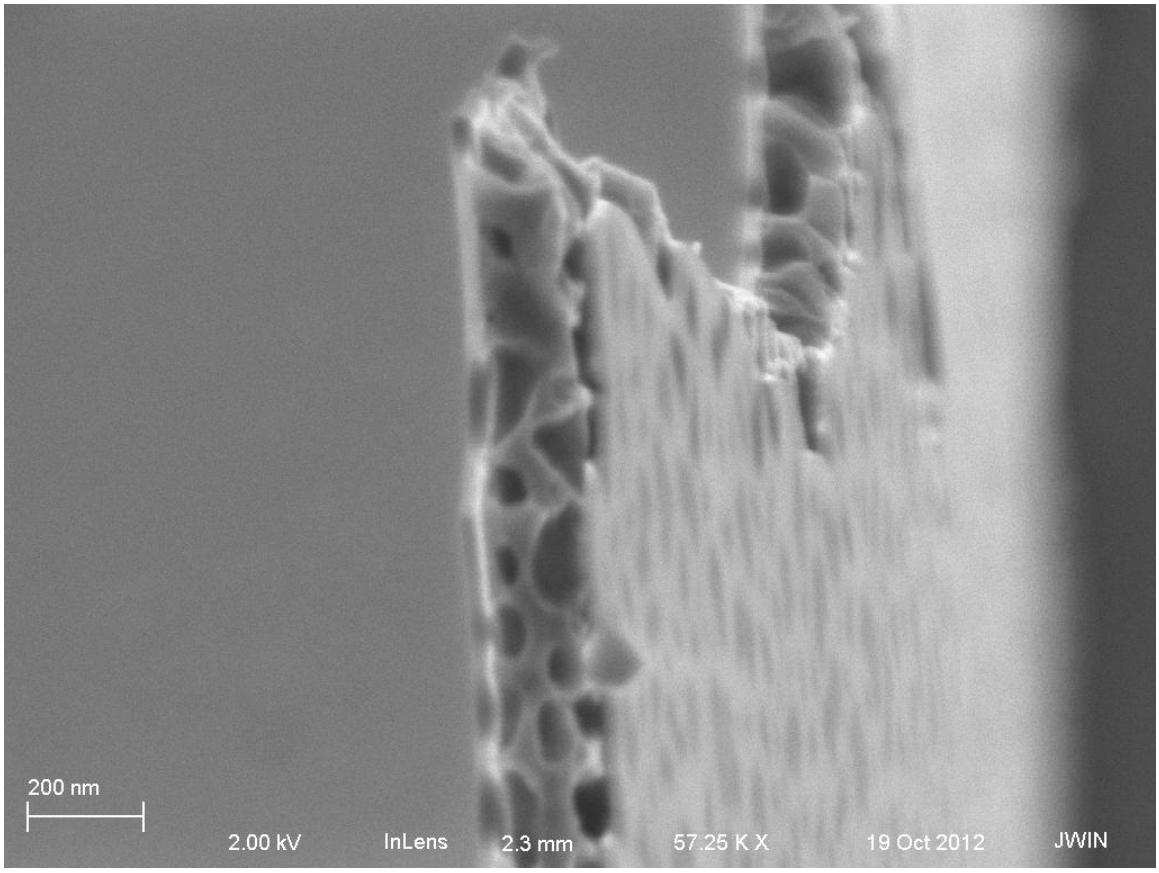

Figure 5-24 Cross-sectional SEM image of 100nm pnc-Si membrane after annealing. Image is credited to Joshua Winans.

The temperature ramp rate determines the crystallization speed of amorphous silicon film, which in turn affects the pore growth speed and the resultant pore shapes. The annealing temperature is assumed to above the silicon crystallization temperature in this discussion. A slow ramp rate leads to a slow crystallization speed, which means more time for silicon atoms to diffuse to nanocrystals from the amorphous matrix. This leads to pore growth process with lots of pore coalesces or split during the slow crystallization process and eventually ends up with lots of pores in irregular shapes. On the contrary, a quick ramp

rate results in a very fast crystallization speed of the amorphous silicon. In this quick crystallization process, there is not enough time for far way silicon atoms to diffuse to silicon nanocrystals to support the growth of nanocrystals. Only silicon atoms from nearby amorphous matrix are able to come to nanocrystals, which leads to the pore growth process with very limited pore coalesces or split. As a result, pores are end up with quite circular shapes.

Capping layer is another factor that affects pore growth during the heating process. It includes capping layer thickness and capping layer materials. In chapter 3 it has been shown capping layer thickness strongly affects the pore growth during the solid-phase crystallization of amorphous silicon films. Thicker capping layer leads to rough interface, which might decrease the diffusivity of silicon atoms and hinder nanocrystal nucleation. As a result the pore growth is suppressed. Capping layer materials also affect the pore growth. In the previous EDS study, it has been shown that Ar is involved in the pore growth process. Ar atoms diffuse together forming bubbles to occupy the porous areas during heating process. Silicon nitride capping layers work as interfacial blockers to prevent the Ar bubbles from escaping the silicon film during annealing. Silicon dioxide capping layers exhibit to be permeable for the Ar atoms and they diffuse out of the silicon film during heating process. This could be the reason attribute to the different pore growth patterns in the NSN and OSO stacks.

5.8 Conclusion

In this chapter, pore formation process in the pnc-Si membrane is studied using ex-situ and in-situ annealing. The ex-situ study on the NSN and OSO stacks shows that silicon crystallization is enhanced in the silicon film in the NSN stack and the associated pore formation is also promoted compared to the OSO stack. The multi-heating experiment confirms that the promoted pore formation in the multi-heating sample is due to the enhanced crystallization of the silicon film. In-situ heating study directly shows the silicon crystallization and pore formation process visually during the heating. It is interesting that pore growth process in the NSN stack shows a pearl-necklace growth pattern while it is not for the OSO stack. The EDS study suggests that Ar molecules are embedded in the amorphous silicon film during sputtering and they diffuse together to form Ar bubbles occupying the porous area in the silicon film during the crystallization process. Silicon nitride capping layers are able to prevent Ar from escaping the silicon film while silicon dioxide layers seem to be permeable for Ar. This may explain the difference in the pore growth pattern in the NSN and OSO stacks. Since pore formation is thermally driven and associated with the silicon crystallization, it can be understood in two stages including void nucleation and pore growth. Nano-voids are nucleated in the silicon film at the interface position and they growth in both vertical and lateral directions as silicon atoms diffuse to silicon nanocrystals from the amorphous matrix. These voids become through pores when their growth spans the entire silicon film in vertical direction. The pore growth is strongly affected by the silicon thickness, temperature ramp rate and capping layers.

Chapter 6 Summary and Future Directions

6.1 Summary

In this thesis, pnc-Si membranes have been extensively studied. The fabrication and characterization processes were first introduced to understand the basic structure and property of this membrane material. Nano-size pores were spontaneously formed in silicon films sandwiched between two silicon dioxide layers during the solid phase crystallization introduced by rapid thermal annealing. Pore formation in the pnc-Si membrane was then studied systematically to understand this unique phenomenon.

To understand the role of the silicon dioxide capping layers during the pore formation process, the effect of variations of silicon dioxide capping films on pore formation was first studied. The result showed that both the top and bottom silicon dioxide films were essential to the pore formation process in pnc-Si membranes. The top SiO_2 layer prevents the silicon film from agglomerating while the bottom SiO_2 layer works as a barrier layer to prevent homoepitaxy from the Si wafer during annealing.

The effect of the employed material as capping layers was studied next. Silicon nitride was incorporated to the sandwich structure, replacing the silicon dioxide capping material. It was found for the first time that nanopores can be formed in the amorphous silicon film ustilizing silicon nitride films as the capping materials during solid phase crystallization. Four different stacks including NSN, NSO, OSN and OSO have been tested.

The result showed that the NSN system produced the highest porosity and pore density after annealing, while the OSO system produced the lowest. The porosity and pore density of the mixed OSN and NSO systems fell between those with matched barrier layers. NSN stacks with different thick silicon films were also studied. Compared to the OSO stack, the NSN stack achieved greater porosity and larger pore size, indicating that pore formation was enhanced in the silicon film and this could be due to the difference in interfacial energy between silicon/silicon nitride and silicon/silicon dioxide.

Ex-situ and in-situ annealing techniques were applied to further study the pore formation process in pnc-Si membranes. The ex-situ study on the NSN and OSO stacks showed that both the silicon crystallization and associated pore formation were enhanced for silicon films in NSN structures as compared to the OSO stack. The multi-heating experiment supported the notion that the pore formation enhancement was due to the enhanced crystallization of silicon film. In-situ heating studies directly showed the silicon crystallization and pore formation process visually during the heating. Pore growth process in the NSN stack demonstrated a pearl-necklace pattern while no clear growth pattern was observed in the OSO stack. The EDS study showed that the embedded Ar molecules during sputtering diffused together to form Ar bubbles occupying the porous area in the silicon film. These Ar bubbles were held in the pores in the silicon film by silicon nitride capping layers but not by silicon dioxide layers. This may explain the different pore growth process in the NSN and OSO stacks.

The pore formation process in the pnc-Si membrane was thermally driven and occurred concurrently with the silicon crystallization. It can be understood in two stages including void nucleation and pore growth. Nano-voids were nucleated in the silicon film at the interface position and they grew in both vertical and lateral directions as silicon atoms from the amorphous matrix diffused to silicon nanocrystals. These voids became through pores when their growth spanned the entire silicon film in vertical direction. The pore growth was strongly affected by the silicon thickness, temperature ramp rate and capping layers.

6.2 Future directions

Some interesting directions are worthwhile to continue according to the results presented in this work. The following sections will discuss the potential research.

6.2.1 Laser annealing

Pores are formed in the silicon film through solid phase crystallization introduced by rapid thermal annealing. The annealing temperature and ramp rate greatly affect the pore morphology, including pore shapes. It has been shown that high ramp rate leads to quite circular pores while low ramp rate produces pores with irregular shapes.

Laser annealing [94-99] would be an interesting research direction for pnc-Si membranes. Generally speaking laser annealing is also a type of rapid thermal annealing with an extreme high ramp rate. The current RTP we used in the lab has ramp rates limited

to 100 ℃/s. We believe laser annealing provides orders of magnitude greater ramp rate than that of the RTP. Some initial work has been carried out at Center for Nanophase Materials Science (CNMS) in Oak Ridge National Lab (ORNL). A KrF excimer pulse laser with 248nm wavelength and full wave half maxim (FWHM) of 25ns has been used for laser annealing test. Figure 6-1 shows TEM image of laser annealed OSO sample. The oxide capping layers are 30nm and the amorphous silicon film is 100nm. Pores with different shapes and sizes are formed in the silicon film after laser annealing with different laser energy densities. Silicon crystals with relatively large grains and grain boundaries can be clearly seen in the TEM images. Higher laser energy density results in bigger pores.

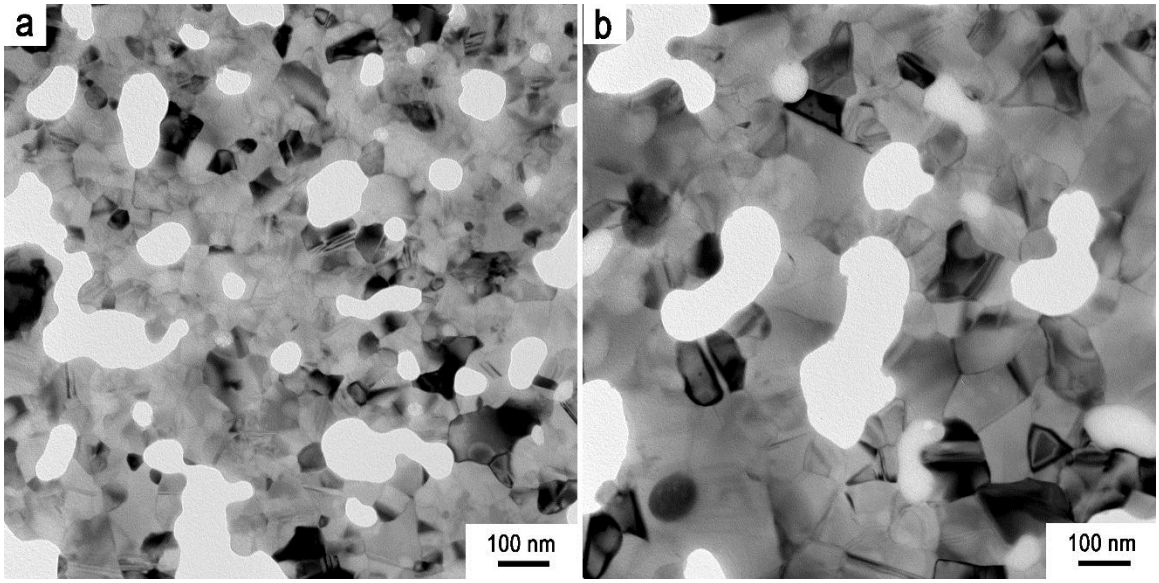

Figure 6-1 TEM image of laser annealed OSO sample with different laser energy densities, (a) 90 mJ/cm2, and (b) 110mJ/cm2.

This initial laser annealing experiment confirms that laser annealing can be used as an alternative rapid thermal annealing method with extremely high ramp rate to introduce

pore formation in the silicon film. This may enable tuning of the pore properties, such as pore size, shape, and pore density, over broader range. This research direction could lead to improved pore properties such as narrow pore size distribution or wider pore size range, for important applications including filtration, gas separation and so on.

6.2.2 Pore formation in other materials

Nanopore formation in the silicon film was original discovered when it was sandwiched by two silicon dioxide layers after rapid thermal annealing [44]. Our latest result showed that nanopores can also be formed when the silicon dioxide layer is replaced by silicon nitride layer in the three-layer stack. This is the first time pore formation in the silicon film has been reported using a different three-layer structure other than the OSO. It indicates the potential that the pore formation might be able to apply to other materials. The emphasis of our present research is to transfer the pore formation to other materials, such as germanium.

Germanium is another important group IV semiconductor material with similar properties to Si. Germanium has a slightly lower melting point (1211K) compared to silicon (1687K). The lattice constant of germanium is 5.66 Å where it is 5.43 Å for silicon. Germanium also has greater electron and hole mobility and smaller band gap compared with silicon. A few studies have been conducted on the porous germanium films. [100-103] So far, anodization and electrochemical etching [3, 16-20], spark processing [21, 22] and

inductively coupled plasma chemical vapor deposition (ICPCVD) [2, 23] have been used to prepare porous Ge films.

It would be very interesting to study whether the pore formation could transfer from the silicon system to germanium system. In the germanium system, different materials can be selected for the capping layers. They include silicon dioxide, silicon nitride layer and germanium oxide. Furthermore, instead of the pure germanium film, germanium and silicon alloy could be another option. This research direction would not only study the feasibility of the pore formation in germanium system, it would also increase our understanding of germanium crystallization.

6.2.3 Strain and stress study

The strain and stress has been shown to greatly affect the crystallization of thin film amorphous silicon [104-105]. Since pore formation is directly associated with silicon crystallization, it is reasonable to assume that strain and stress plays a role in the formation of pores in pnc-Si membranes. As a result, a future study on strain and stress would be very helpful to future develop our currently understanding on nanopore formation.

There are several methods to characterize the stress in thin films, such as x-ray diffraction (XRD) [106], and curvature measurements [107]. Initial stress should be measured after deposition of the three-layer stack (either the NSN or OSO). During a rapid thermal annealing process, the silicon film undergoes a phase transition from amorphous to nanocrystalline. As a result, the stress in the three-layer stack changes after annealing.

To systematically study the stress effect on pore formation, different stress values due to different annealing temperatures should be measured after annealing. This would result in a comprehensive study between the stresses and pore characteristics to further our understanding of the effect of strain and stress on pore formation.

6.2.4 Ar-free silicon deposition

Ar bubbles have been shown to occupy porous areas in pnc-Si membranes after annealing and they are held by the capped nitride layers in the EDS study. They diffuse out of the silicon film when the capped nitride layers are removed. Since Ar bubbles occupy nanopores during the pore formation, it would be very informative to estimate the gas pressure of the Ar bubbles in the pores.

A rough estimation of the Ar bubble pressure has been conducted using the idea gas law, see equation 6-1

$$PV = nRT \qquad (6\text{-}1)$$

In this equation, P is the absolute pressure of the gas, V is the volume of the gas, n is the amount of substance of gas (measured in moles), R is the ideal, or universal, gas constant, and T is the absolute temperature of the gas. Since Ar bubbles occupy the porous areas in the pnc-Si membrane, the porosity of the silicon film can be used to represent the volume ratio of the Ar bubbles to the silicon film. The amount of the Ar can be calculated using the atomic percentage result from the EDS study. By using a 20% porosity and a 4%

Ar atomic percentage, the average pressure of the Ar bubbles inside the pores is estimated to be on the order of 1000 atmosphere pressure. This rough estimation suggests that the Ar bubbles inside nanopores are under a very high pressure. It is possible that Ar is on longer in gaseous phase under such a high pressure. Future research with a more accurate model to calculate the Ar pressure would be very instructive to reveal how the Ar atoms are evolved during the formation of nanopores in the pnc-Si membrane.

Meantime, it is necessary to further the study of pore formation using other plasma gas sources than Ar. Since the Ar bubbles are directly involved in the pore formation, it is likely that other embedded plasma source atoms may work similarly as to that of the Ar.

A direct way is to replace the sputtering gas source from Ar to other noble gas such as Ne or Kr. Either case would introduce new embedded defect atoms (Ne or Kr) in the silicon film during sputtering. An in-situ heating or RTA process should be used to crystallize the sputtered Ar-free Si film sandwiched by either nitride or oxide to verify whether nanopores could be formed in the silicon film after annealing. To make fair comparison of the results between the Ar-embed and Ar-free silicon films, several requirements should be met. The first one is that silicon films should be of the same thickness. Other requirement includes that both the capping layers and annealing condition should be identical in the two systems. This result would be very useful and informative to verify the principle of Ar during the pore formation in pnc-Si membranes.

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